TB-6S-LX150T-IMG2
Hardware User Manual

Rev.1.02

Revision History

Version	Date	Description	Publisher
Rev.1.00	2011/01/20	Initial Release.	Yoshioka
Rev1.01	2011/02/17	Modified register number of TDI/TDO connection of FMC Modified configuration LED numbers	Yoshioka
Rev1.02	2011/03/15	Brash up all of sections.	Yoshioka

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Introduction

Thank you for purchasing the **TB-6S-LX150T-IMG2** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, and then always keep it handy.

SAFETY PRECAUTIONS

Be sure to observe these precautions

Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to assure correct use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to always keep it handy.**

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
Warning	Indicates the possibility of serious injury or death if the product is handled incorrectly.
Caution	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

Warning	
	In the event of a failure, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.
	If an unpleasant smell or smoking occurs, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.
	Do not disassemble, repair or modify the product. Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	Do not touch a cooling fan. As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.
	Do not place the product on unstable locations. Otherwise, it may drop or fall, resulting in injury to persons or failure.
	If the product is dropped or damaged, do not use it as is. Otherwise, a fire or electric shock may occur.
	Do not touch the product with a metallic object. Otherwise, a fire or electric shock may occur.
	Do not place the product in dusty or humid locations or where water may splash. Otherwise, a fire or electric shock may occur.
	Do not get the product wet or touch it with a wet hand. Otherwise, the product may break down or it may cause a fire, smoking or electric shock.
	Do not touch a connector on the product (gold-plated portion). Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Caution	
	Do not use or place the product in the following locations. • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Staticky locations • Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
	Do not place heavy things on the product. Otherwise, the product may be damaged.

■ Disclaimer

This product is an evaluation board for Xilinx FPGA, Spartan6. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

(1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
(2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
(3) Use of this product against the instructions given in this manual.
(4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

(1) Erasure or corruption of data arising from use of this product.
(2) Any consequences or other abnormalities arising from use of this product, or
(3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.

1. Related Documents and Accessories

Related documents:

All documents and reference designs relating to this board are available only for purchasing customers and can be downloaded from our website at Tokyo Electron Device Ltd. TED SUPPORT WEB (http://ppg.teldevice.co.jp/eng/index.htm).

Mounting parts

7 x rubber foots, 14 x M3 X 6mm screws and 7 x M3 X 10mm spacers

Accessories

Option board spacer set:

6 x M2.6 X 10mm spacers (Duracon) and 12 screws with Duracon washers

MMCX cable set:

2 x MMCX-SMA cables (Samtec RF174-03SP1-01SP1-0400)

2 x MMCX-MMCX cables (Samtec RF174-03SP1-03SP1-0400)

AC adaptor

1 x AC adaptor (Akizuki Denshi: LTE(GFP)451DA-1238 or equivalents)

2. Overview

The TB-6S-LX150T-IMG2 DDR3, 8 channel GTP, and Xilinx Spartan®-6 evaluation board forms the base for numerous Spartan-6 development platforms including the Consumer Video Kit 2.0.

3. Feature

- XC6SLX150T-3FG900 FPGA
- 1 x VITA-57 standard FPGA Mezzanine Card (FMC) High Pin Count (HPC) connector
- 2 x FMC Low Pin Count (LPC) connectors.
  Due to limitations on the number of FPGA pins, all defined FMC standard signals are not connected. For more information, refer to the Connector Pinout Tables in this manual on pages 24, 31, and 35.
- 3 x DDR3 SDRAM (Chip): Micron MT41J64M16LA-15E(or equivalent) (1 Gbits 800Mbps)
- 4 x 4 LVDS crosspoint switch
- Clocks (see Figure 7-7 Clock Distribution Diagram)
  - Multiple onboard clock sources (200 MHz, 27 MHz, 74.25 MHz)
  - User populated clock chip in 8-pin dip
  - External clock sources via single ended and differential MMCX connections with clock cleaners
  - PLL clock generator programmable from the FPGA
  - MMCX clock output
  - DIP switch selectable MGT clock source selection
- Push button switches, dip switches and pin headers
- LEDs
- USB connection to a PC (via USB-UART conversion device) for character based terminal I/O
- 128 Mbit SPI Flash configuration ROM
- TI TPS 386000 Voltage Supervisor

4. Block Diagram

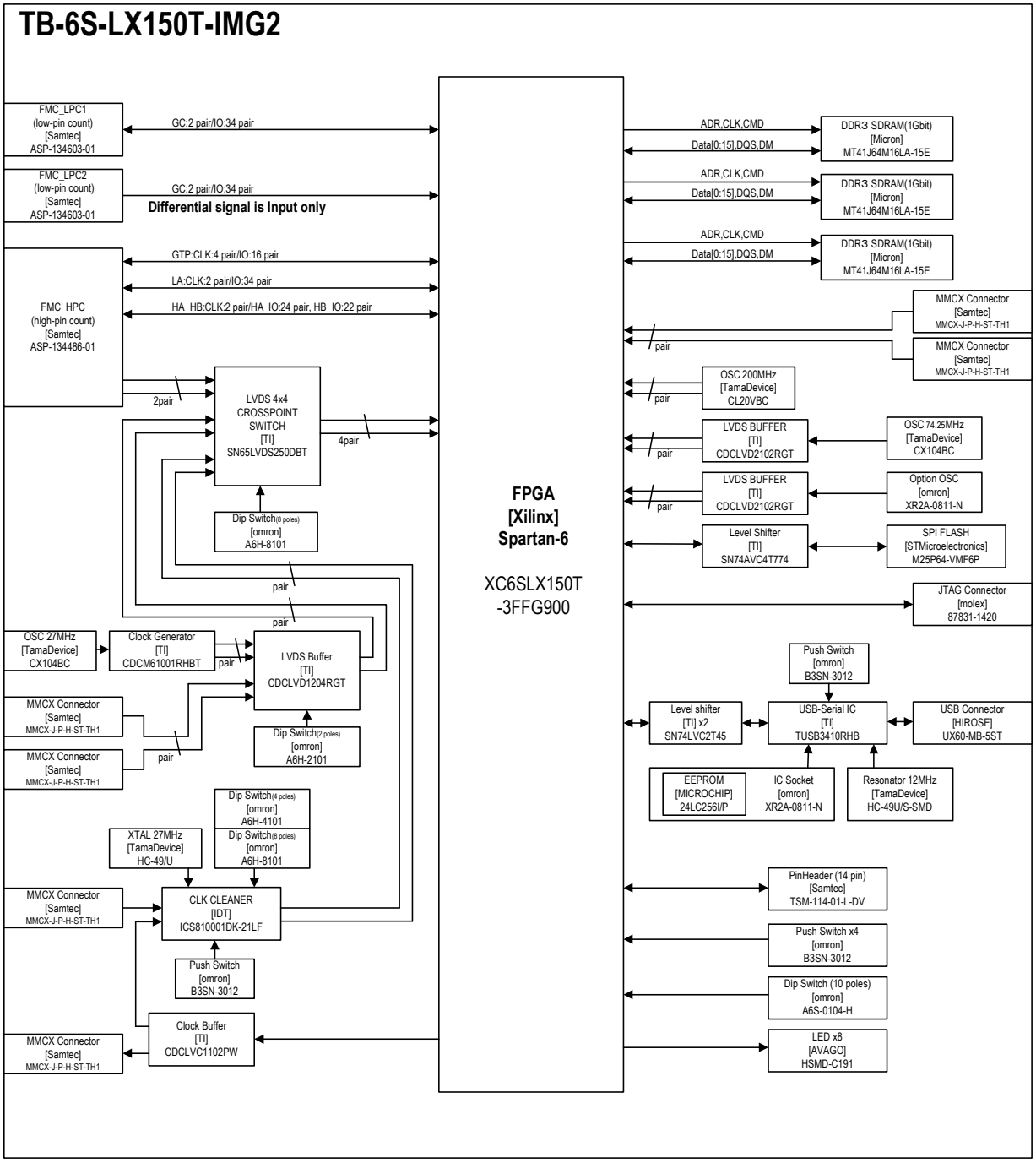


Figure 4-1 Block Diagram

5. External view of board

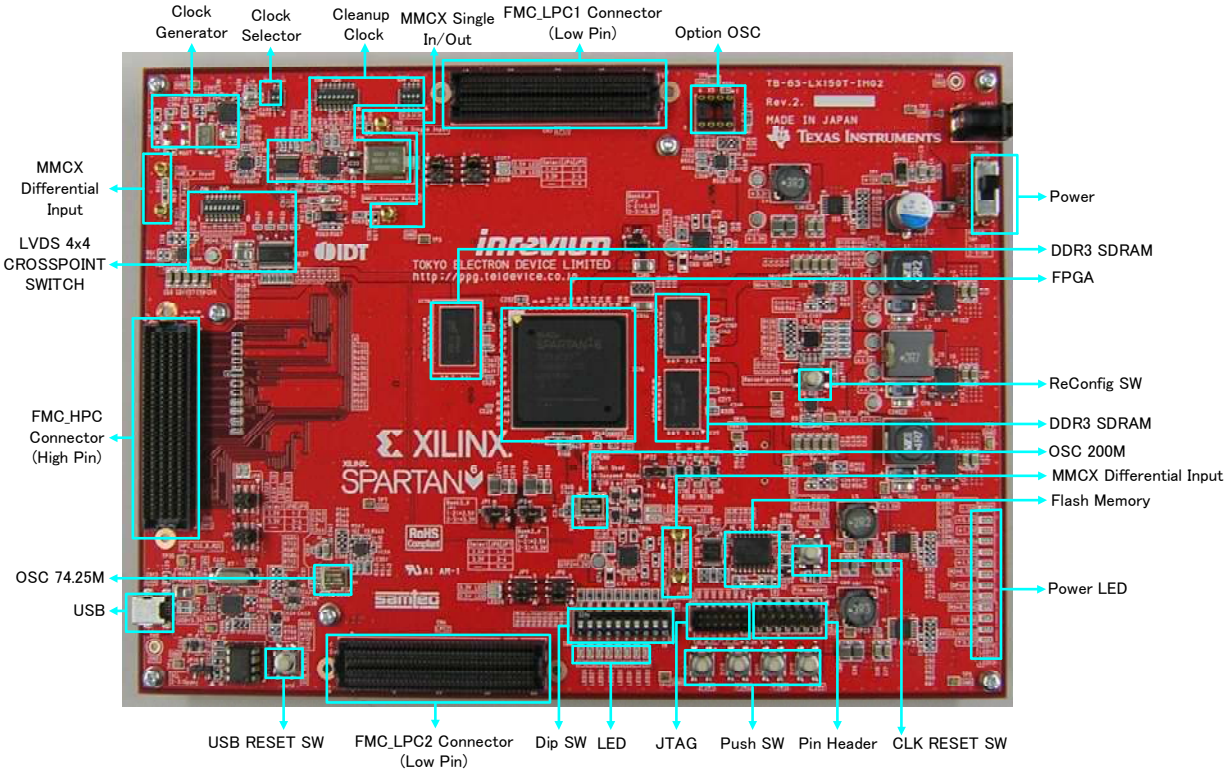


Figure 5-1 component side

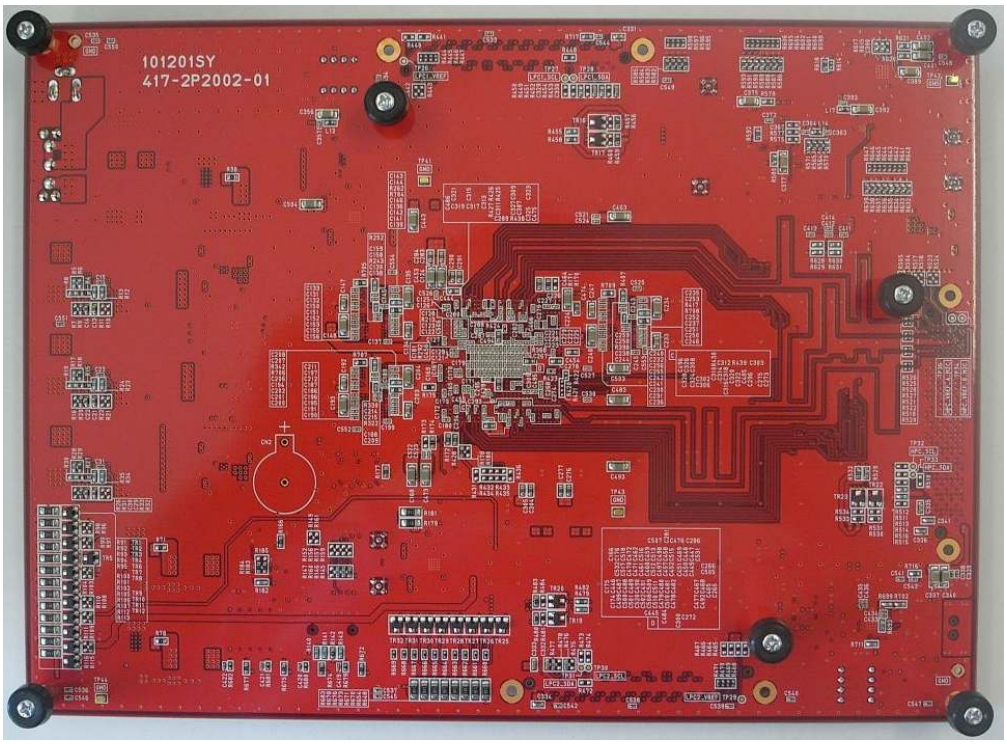


Figure 5-2 Solder side

6. Board Specifications

External Dimensions:	W: 240.00mm x H: 175.00mm
Number of Layers:	12 layers
Board Thickness:	1.6mm
Material:	FR-4
FPGA:	Xilinx XC6SLX150T-3FGG900
PROM:	ST Micro M25P64-VMF6P
FMC Connector (High-Pin):	Samtec ASP-134486-01
FMC Connector (Low-Pin):	Samtec ASP-134603-01
DDR2 SDRAM:	Micron MT41J64M16LA-15E
MMCXConnector:	Samtec MMCX-J-P-H-ST-TH1

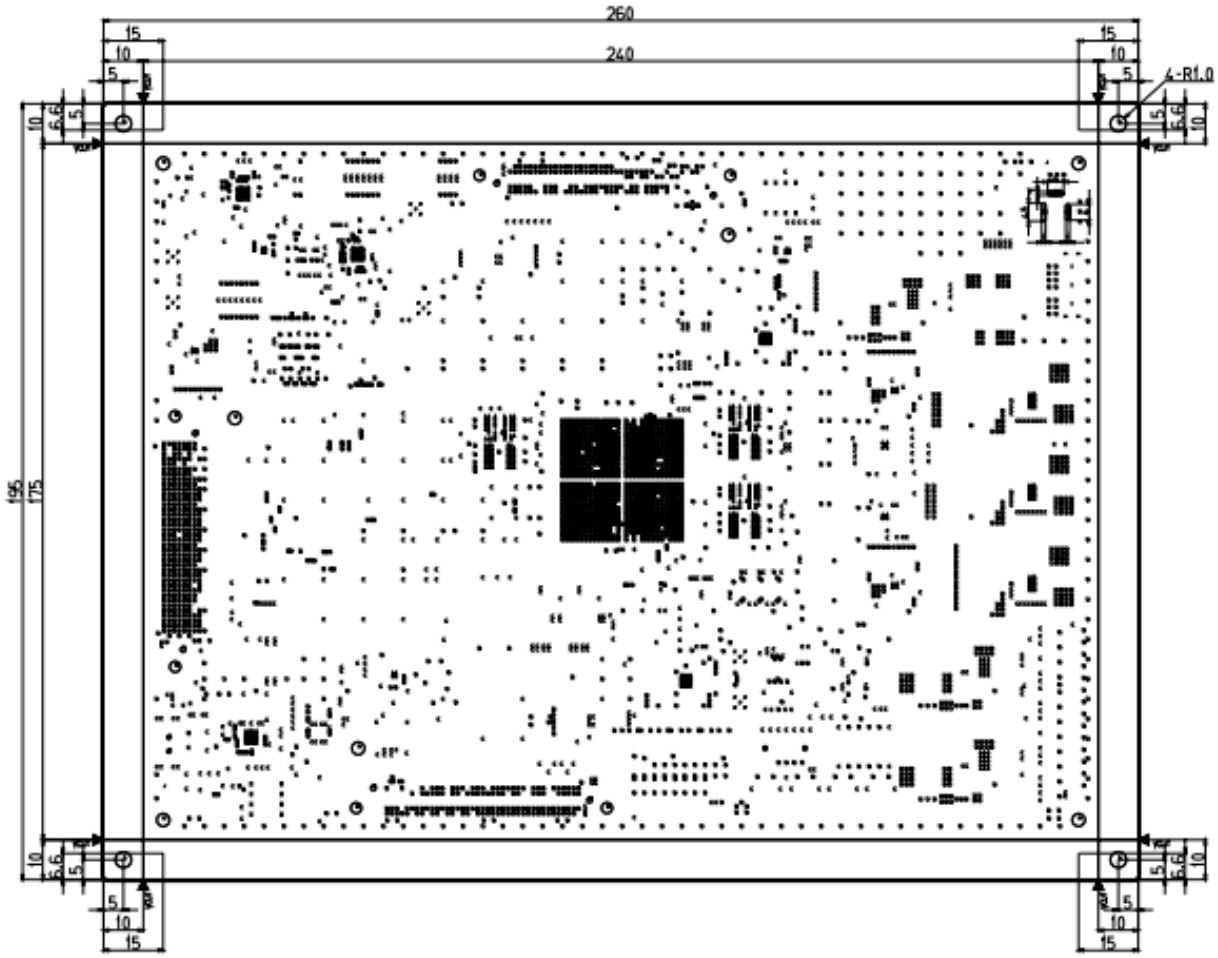


Figure 6-1 TB-6S-LX150T-IMG2 board dimensions

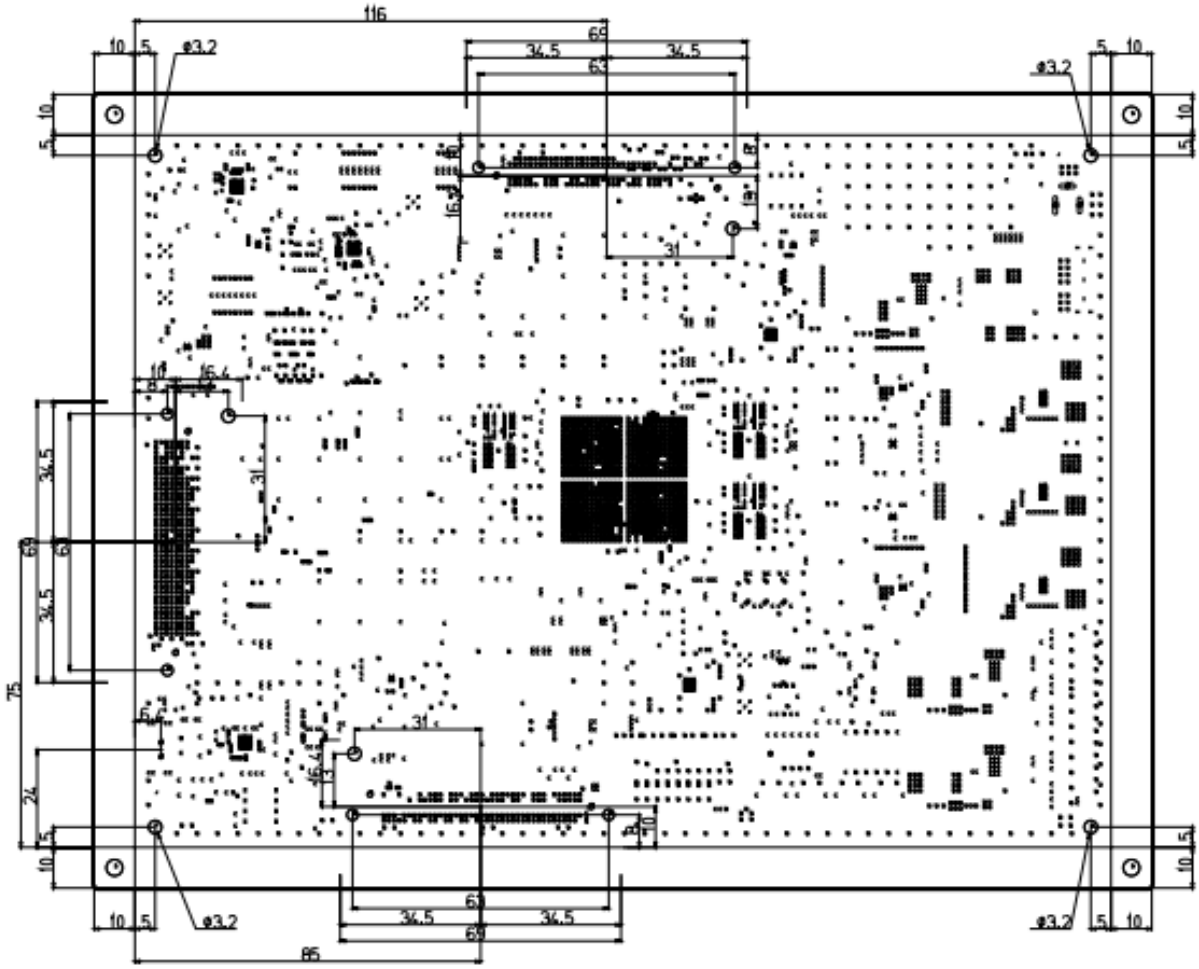


Figure 6-2 Hole positions

7. Description of Components

7.1. Power Supply Structure

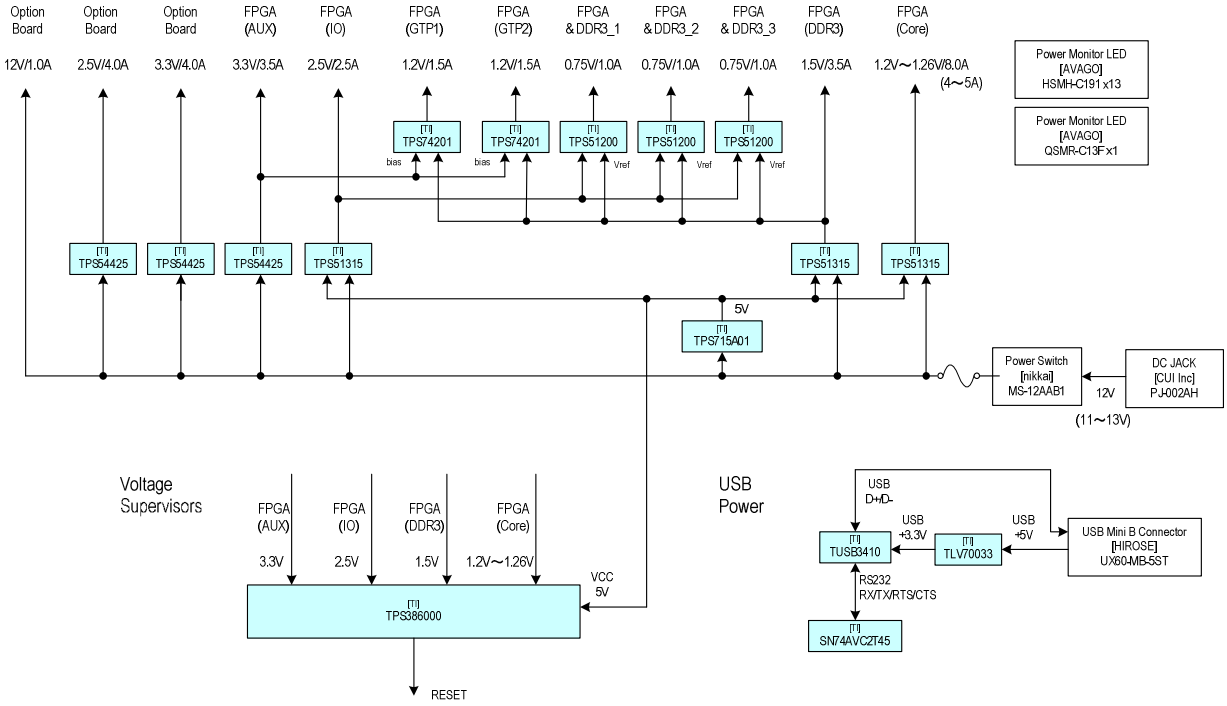


Figure 7-1 Power Supply Structure

Power Input

Power is supplied through the AC adaptor..

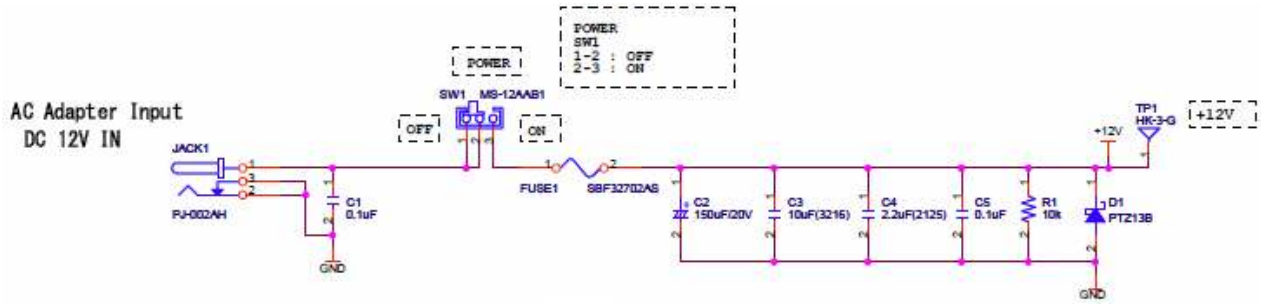


Figure 7-2 Structure of the AC adapter input power connection

Power Status LED

The board provides 13 LEDs to signal the correct operational status of each voltage rail.

Table 7-1 Power status LEDs

Voltage	LED	Description	Color
12V	LED1	12V power supply	Blue
5.0V	LED2	Power for 1.2/1.5/2.5V	Red
1.2V	LED3	Power for FPGA VCCINT	Red
M1+0.75V	LED4	Power for FPGA VREF(DDR3)	Red
2.5V	LED5	Power for FPGA VCCIO	Red
1.5V	LED6	Power for FPGA VCCIO	Red
M2+0.75V	LED7	Power for FPGA VREF(DDR3)	Red
OP+2.5V	LED8	Power for FMC	Red
1.2V_A1	LED9	Power for MGT AVCC1/AVTT1	Red
M3+0.75V	LED10	Power for FPGA VREF(DDR3)	Red
OP+3.3V	LED11	Power for FMC	Red
1.2V_A2	LED12	Power for MGT AVCC2/AVTT2	Red
3.3V	LED13	Power for FPGA VCCIO	Red

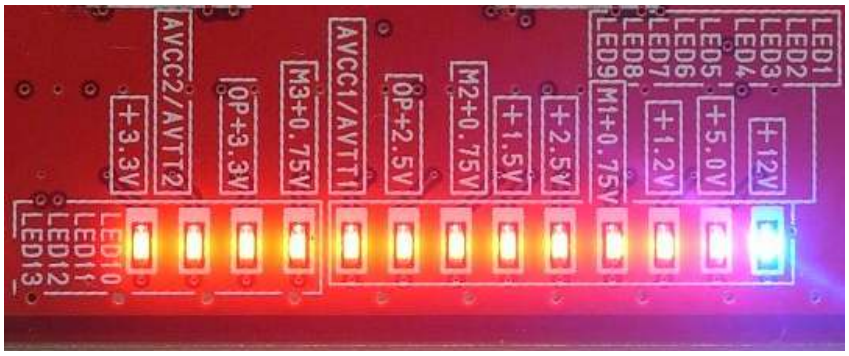


Figure 7-3 Power status LED

FPGA Bank Voltage Selection

Various peripheral devices are connected to FPGA as shown in following figure. The FMC connectors allow the developers to select an appropriate FPGA Bank voltage (VCCIO) by setting the onboard jumpers (JP1, 2 and 3) to meet the voltage requirements (3.3V or 2.5V) for the connected interfaces.

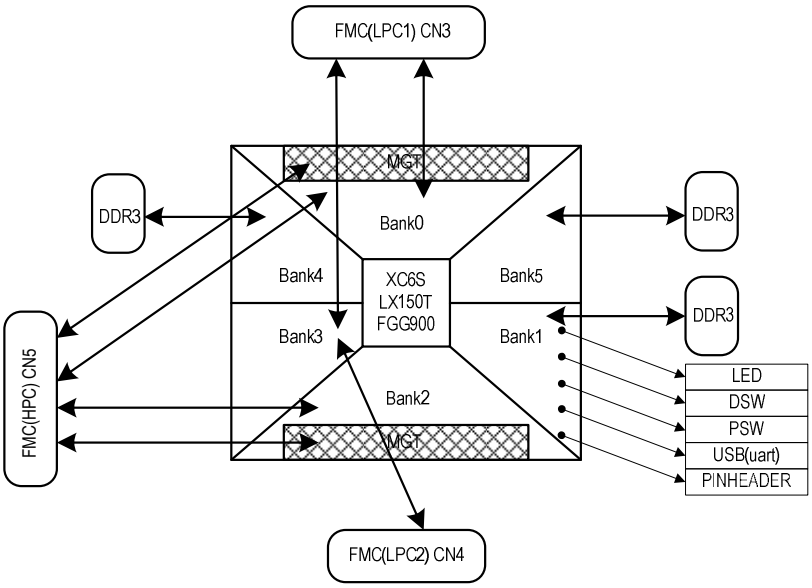


Figure 7-4 FPGA Banks and Peripheral Devices

Table 7-2 FPGA Banks and Corresponding Devices

Bank	Function	Voltage	Voltage Selection		
			SEL	2.5V	3.3V
Bank0	FMC_HPC(CN5)	Selectable (3.3V/2.5V)	JP2	1-2	2-3
Bank1	DDR3,DSW,LED,PSW,USB	1.5V	-	-	-
Bank2	FMC_HPC(CN5)	Selectable (3.3V/2.5V)	JP3	1-2	2-3
Bank3	FMC_LPC1(CN3), FMC_LPC2(CN4)	Selectable (3.3V/2.5V)	JP1	1-2	2-3
Bank4	DDR3	1.5V	-	-	-
Bank5	DDR3	1.5V	-	-	-

Selectable voltage is initially 2.5V settings

Bank0 Bank2/3

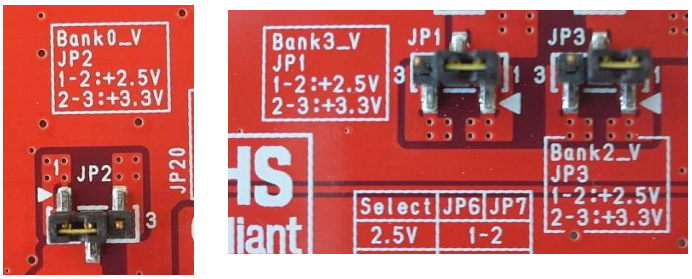


Figure 7-5 Location of FPGA Bank Voltage Selection

7.2. Oscillator

The board provides the following clock sources.

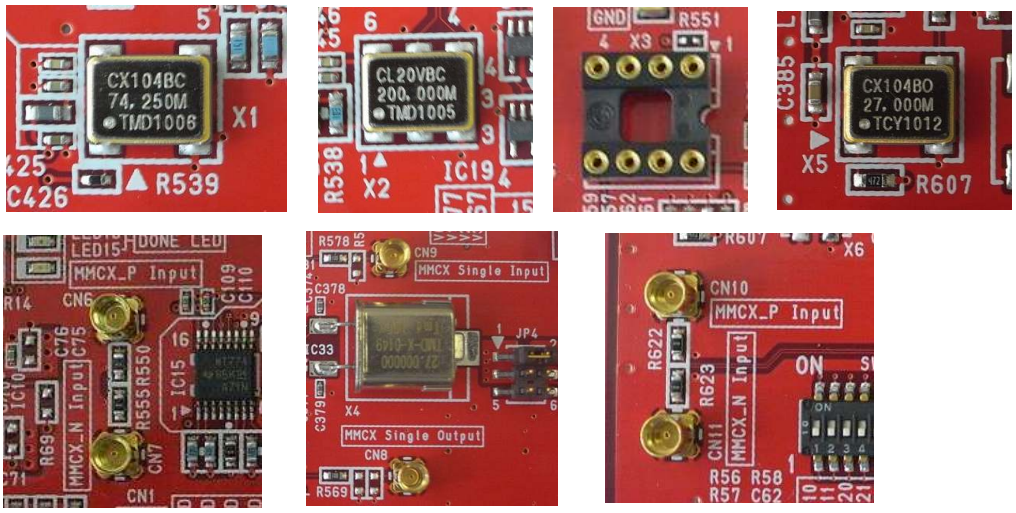


Figure 7-6 Clock Sources

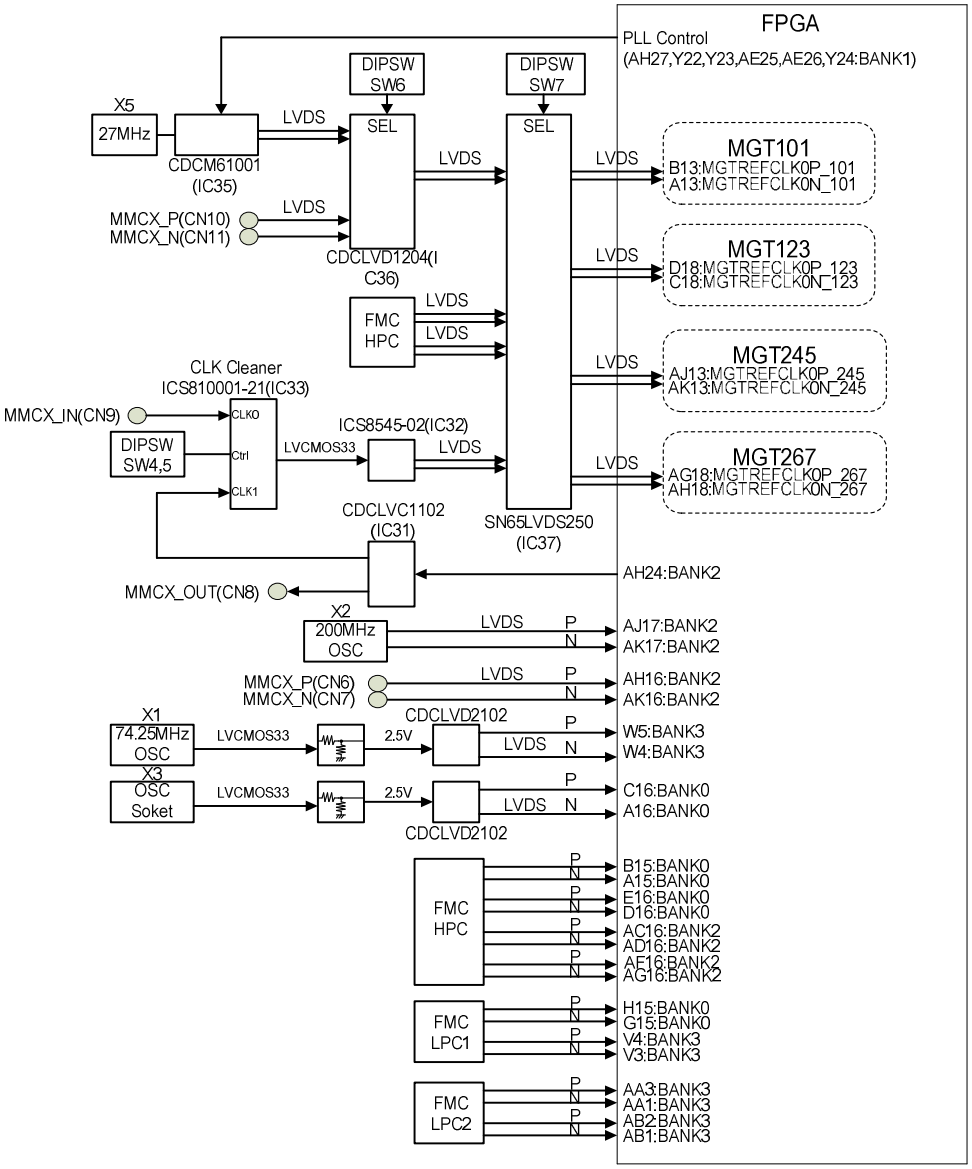


Figure 7-7 Clock Distribution Diagram

Table 7-3 Details of On board Oscillator

connection	name	I/F	FPGA PIN	Remakes
X1	CLK74.25M_P/N	LVDS	W5/W4	Single ended to differential signal buffer
X2	CLK200M_P/N	LVDS	AJ17/AK17	DDR3(IDelay) clock
X3	CLK_OPTION_P/N	LVDS	C16/A16	Single ended to differential signal buffer
CN6/7	MMCX_P/N	LVDS	AH16/AK16	MMCX external clock
IC32 (FB_CLEANUP_CLKP/N) or CN5(HPC_GBTCLK0_M2C_P/N) or CN5(HPC_GBTCLK1_M2C_P/N) or IC36(PLL/MMCX_CLKP/N)	HPC_CLK_M101_P/N HPC_CLK_M245_P/N HPC_CLK_M123_P/N HPC_CLK_M267_P/N	LVDS	B13/A13 AJ13/AK13 D18/C18 AG18/AH18	MGT reference clock
FMC_HPC(CN5)	HPC_CLK0_M2C_P/N	LVDS	B15/A15	HPC_LA interface clock
FMC_HPC (CN5)	HPC_CLK1_M2C_P/N	LVDS	E16/D16	HPC_LA interface clock
FMC_HPC (CN5)	HPC_CLK2_M2C_P/N	LVDS	AC16/AD16	HPC_HA_HB interface clock
FMC_HPC (CN5)	HPC_CLK3_M2C_P/N	LVDS	AF16/AG16	HPC_HA_HB interface clock
FMC_LPC1(CN3)	LPC1_CLK0_M2C_P/N	LVDS	V4/V3	LPC1interface clock
FMC_LPC1(CN3)	LPC1_CLK1_M2C_P/N	LVDS	H15/G15	LPC1interface clock
FMC_LPC2(CN4)	LPC2_CLK0_M2C_P/N	LVDS	AA3/AA1	LPC2 interface clock
FMC_LPC2(CN4)	LPC2_CLK1_M2C_P/N	LVDS	AB2/AB1	LPC2 interface clock

Supplementary explanation: HPC_CLK*_M2C_P/N and LPC*_M2C_P/N can be used for single-end signal.

7.3. MGT reference clock

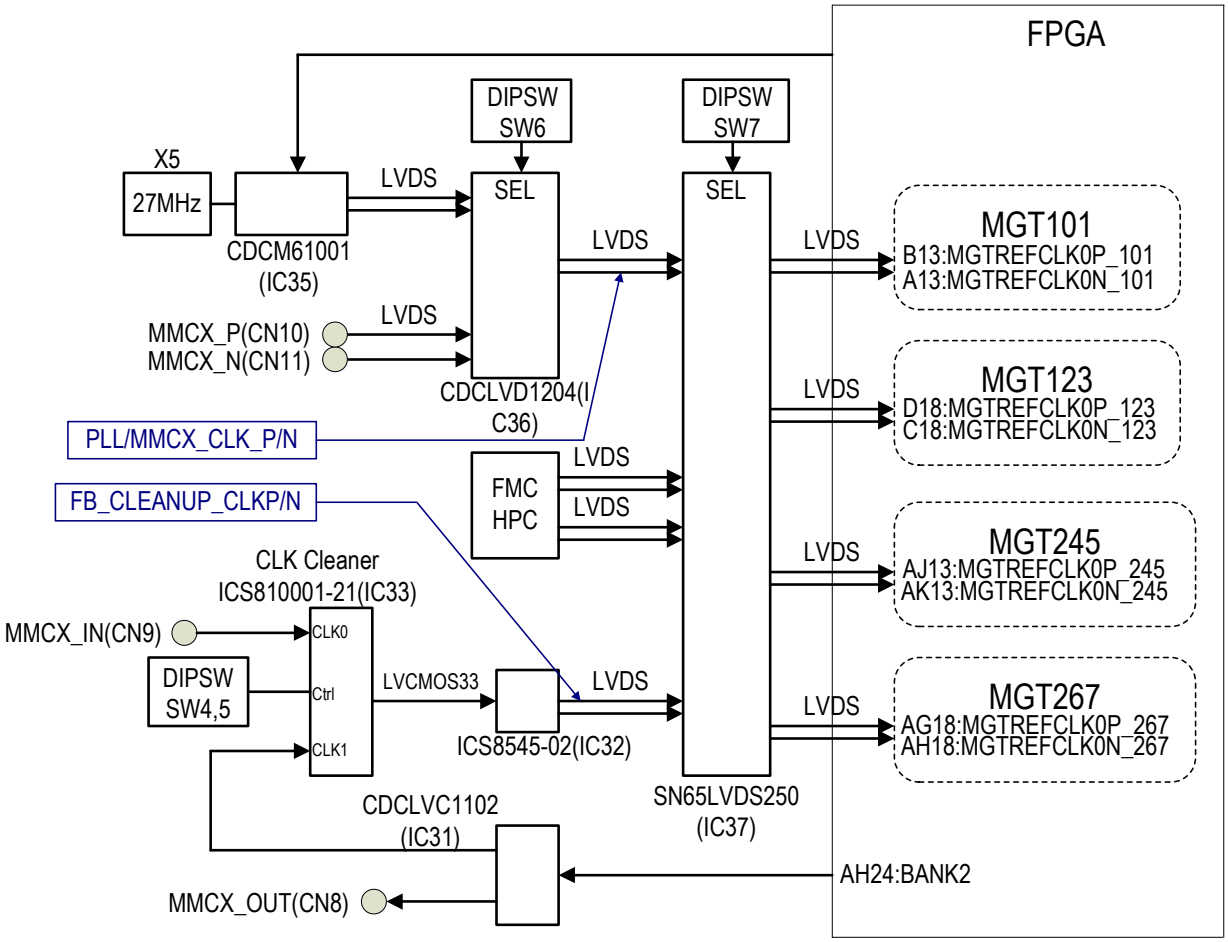


Figure 7-8 MGT reference clock structure

7.3.1. PLL/MMCX_CLK_P/N

PLL/MMCX_CLK_P/N is input clock for “SN65LVDS250DBT”. This is selected MMCX_P/N(CN10, 11) or a clock generator(IC35: CDCM61001RHBT) by clock selector(IC36: CDCLVD1204RGT) and SW6(DIP-SW)

The clock generator (IC35) uses 27MHz OSC(X5) for its master clock.

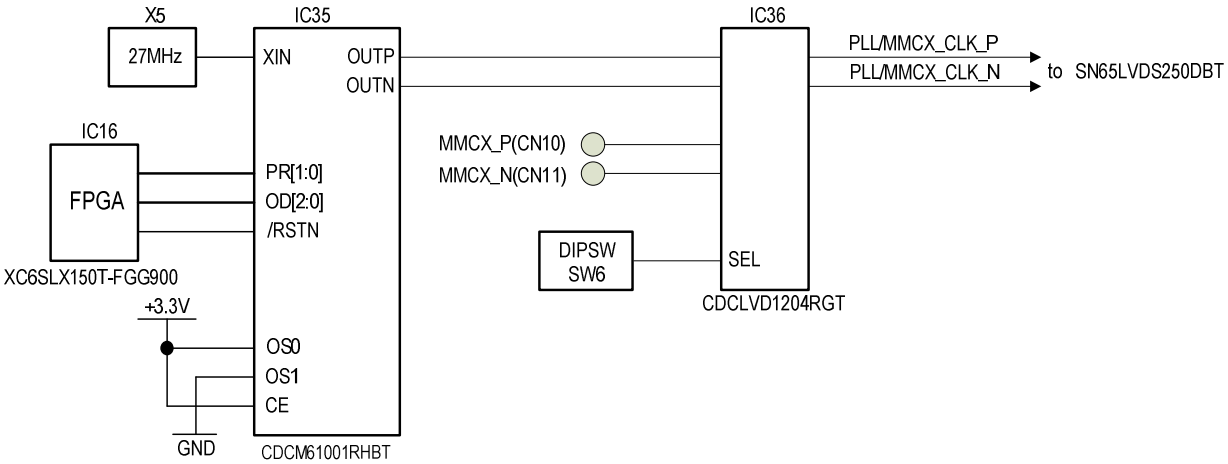


Figure 7-9 PLL/MMCX_CLK_P/N structure

Table 7-4 PLL/MMCX_CLK_P/N setting

SW6		Selected clock	
1	2	OUTP	OUTN
OFF	OFF	L	H
ON	OFF	MMCX	
OFF	ON	PLL Clock	
ON	ON	PLL Clock	

7.3.1.1. Clock Generator(CDCM61001RHBT)

This board uses a low jitter clock generator(TI CDCM61001RHBT). For more detail settings, please refer to the data sheet of CDCM61001RHBT.

The output frequency and reset of clock generator is controlled by FPGA. It has 27MHz OSC for XIN.

Table 7-5 Clock Generator(CDCM61001RHBT)IC settings

Signal	FPGA Pin No.	Used for
PR[1]	AE26	Setting for pre-scaler divider and feedback divider
PR[0]	AE25	
OD[2]	Y23	Setting for output divider
OD[1]	Y22	
OD[0]	AH27	
RSTN	Y24	Reset from FPGA
OS[1:0]	-	OS[1:0] = 01 fixed
CE	-	CE = 1fixed

Calculation for frequency of clock output

Fout = VCO / Prescaler Divider / Output Divider

For example: Generate 135MHz clock output.

Conditions: Input clock is 27MHz (VCO=2025)

PR[1:0] = OFF,ON (Prescaler Divider = 5, Feedback Divider = 15)

OD[2:0] = OFF,ON,OFF(Output Divider = 3)

7.3.2. FB_CLEANUP_CLKP/N

"FB_CLEANUP_CLKP/N" is differential input clock signal for the "SN65LVDS250DBT". This differential signal is converted from single-ended to differential by IC32. The single-ended clock is generated by the IDT video clock generator (ICS810001DK-21LF).

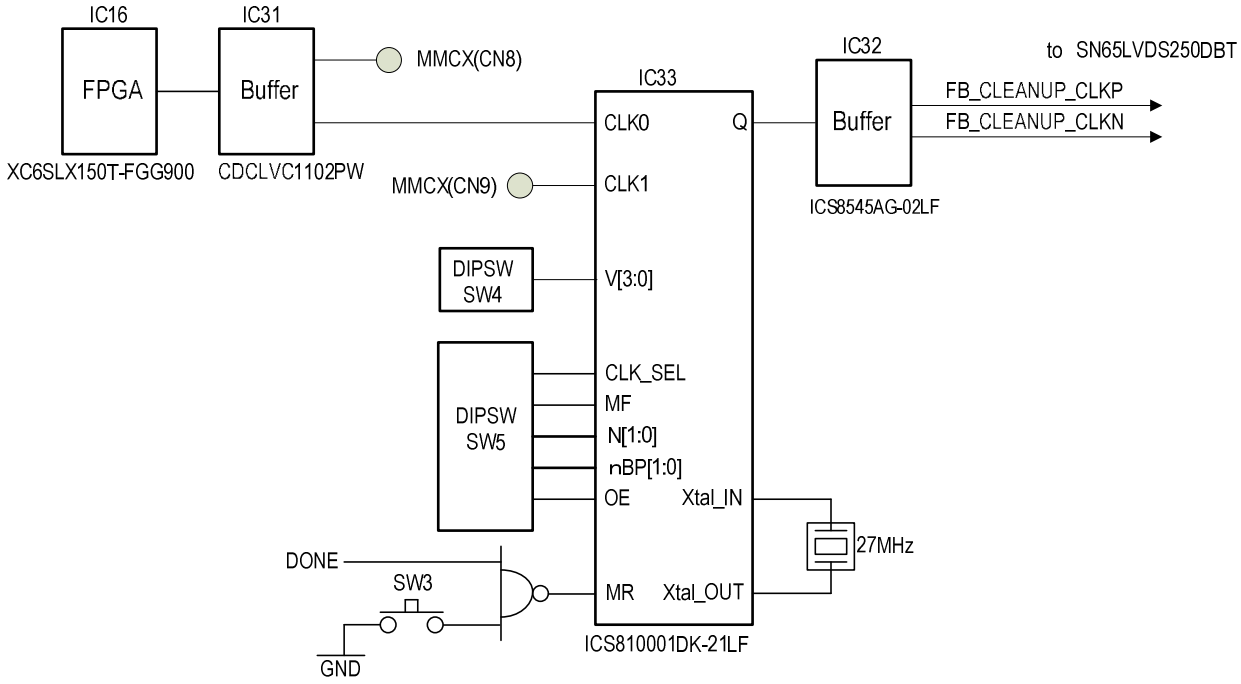


Figure 7-10 FB_CLEANUP_CLKP/N structure

7.3.2.1. Clock Generator(ICS810001DK-21LF)

The board provides an onboard video clock generation circuit using the IDT ICS810001DK-21LF. For details about setting clock frequencies, refer to the corresponding IDT data sheet.

This device accepts a clock sourced from the FPGA (AH24 pin) or from an external MMCX connector (CN9). The clock source selection is made via DIP switch SW5. The user selects the output clock frequency generated by this IDT video clock generator PLL via DIP switch SW5. The XTAL_IN is connected a 27MHz oscillator. A reset to this device occurs during power-up or by pressing pushbutton SW3.

Table 7-6 Clock Generator (ICS810001DK-21LF) IC settings

Signal	SW No.	SW bit	Purpose
V[3:0]	SW4	bit[4:1]	Input clock setting
CLK_SEL	SW5	bit[1]	Input clock selection (ON=MMCX/OFF=FPGA)
MF		bit[2]	PLL coefficient
N[1:0]		bit[4:3]	Frequency dividing value: 00=4 / 01=8 / 10=12 / 11=18
nBP[1:0]		bit[6:5]	Output clock generation block structure setting
OE		bit[7]	Output clock enable (ON=Enable)

Output clock formula in nBP[1:0]=11(ON,ON):

Fout = (in_CLK / P) x M x MF / N

Example: 148.5MHz output

Condition: Input clock: 27MHz (V[3:0]=ALL OFF=(P=1000)=(M=1000))

MF=OFF (x22)

N[1:0]=OFF,OFF (divide-by-4 frequency)

7.3.3. MGT reference clock selector

MGT reference clocks are selected by LVDS 4x4 crosspoint switch IC37 (TI: SN65LVDS250DBT). 4 clock sources are selected by SW7.

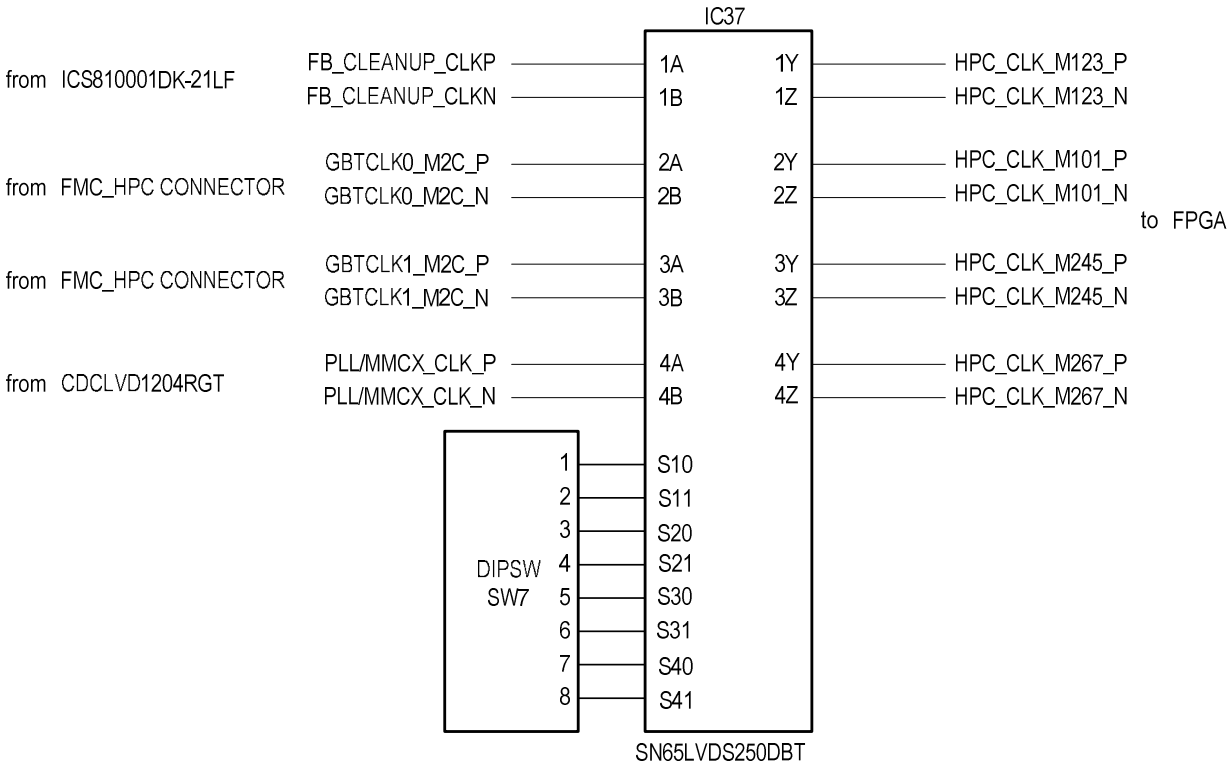


Figure 7-11 MGT reference clock selector IC

Table 7-7 MGT reference clock settings

OUTPUT CHANNEL 1			OUTPUT CHANNEL 2			OUTPUT CHANNEL 3			OUTPUT CHANNEL 4		
S10	S11	1Y/1Z	S20	S21	2Y/2Z	S30	S31	3Y/3Z	S40	S40	4Y/4Z
OFF	OFF	1A/1B	OFF	OFF	1A/1B	OFF	OFF	1A/1B	OFF	OFF	1A/1B
OFF	ON	2A/2B	OFF	ON	2A/2B	OFF	ON	2A/2B	OFF	ON	2A/2B
ON	OFF	3A/3B	ON	OFF	3A/3B	ON	OFF	3A/3B	ON	OFF	3A/3B
ON	ON	4A/4B	ON	ON	4A/4B	ON	ON	4A/4B	ON	ON	4A/4B

For example: Selecting FB_CLEANUP_CLKP/N to HPC_CLK_M123/245_P/N
and HPC_GBTCLK0_M2C_P/N to HPC_CLK_M101/267_P/N.

SW7	
1: OFF	2: OFF
3: OFF	4: ON
5: OFF	6: OFF
7: OFF	8: ON

7.4. FMC Connector Interface

The board provides 3 Samtec FMC connectors.

High-Pin Count : 1 (CN5)

Low-Pin Count : 2 (CN3, CN4)

Figure 7-12 and Figure 7-13 show the VITA-57 High-Pin Count and Low-Pin Count FMC pinouts respectively.

Notice: Not all pins of the HPC and LPC connectors are connected to the FPGA.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure 7-12 VITA-57 Standard High-Pin Count Connector

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure 7-13 VITA-57 Standard Low-Pin Count Connector

7.4.1. HPC (High-Pin Count)

The FMC high-pin count connector connects the following number of signals to the FPGA:

High Speed: 8 ch(TX), 8 ch (RX) and 2 clocks

Low Speed: LA 34 pair (68 single-end) and 2 clocks.

HA 24 pair (48 single-end) and 2 clocks (common of HA/HB).

HB 22 pair (44 single-end).

Table 7-8 HPC Column A & B Pin to FPGA Pin Assignment

Bank No.	Pin No.	A		B	PinNo.	Bank No.
		GND	1	RES1		
MGTRXP1_101	D12	DP1_M2C_P	2	GND		
MGTRXN1_101	C12	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P		
		GND	5	DP9_M2C_N		
MGTRXP0_123	D20	DP2_M2C_P	6	GND		
MGTRXN0_123	C20	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P		
		GND	9	DP8_M2C_N		
MGTRXP1_123	D22	DP3_M2C_P	10	GND		
MGTRXN1_123	C22	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	AG22	MGTRXP1_267
		GND	13	DP7_M2C_N	AH22	MGTRXN1_267
MGTRXP0_245	AG10	DP4_M2C_P	14	GND		
MGTRXN0_245	AH10	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	AG20	MGTRXP0_267
		GND	17	DP6_M2C_N	AH20	MGTRXN0_267
MGTRXP1_245	AG12	DP5_M2C_P	18	GND		
MGTRXN1_245	AH12	DP5_M2C_N	19	GND		
		GND	20	*1 GBTCLK1_M2C_P	*1	*1
		GND	21	*1 GBTCLK1_M2C_N	*1	*1
MGTTXP1_101	B11	DP1_C2M_P	22	GND		
MGTTXN1_101	A11	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P		
		GND	25	DP9_C2M_N		
MGTTXP0_123	B21	DP2_C2M_P	26	GND		
MGTTXN0_123	A21	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P		
		GND	29	DP8_C2M_N		
MGTTXP1_123	B23	DP3_C2M_P	30	GND		
MGTTXN1_123	A23	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	AJ23	MGTTXP1_267
		GND	33	DP7_C2M_N	AK23	MGTTXN1_267
MGTTXP0_245	AJ9	DP4_C2M_P	34	GND		
MGTTXN0_245	AK9	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	AJ21	MGTTXP0_267
		GND	37	DP6_C2M_N	AK21	MGTTXN0_267
MGTTXP1_245	AJ11	DP5_C2M_P	38	GND		
MGTTXN1_245	AK11	DP5_C2M_N	39	GND		
		GND	40	RES0		

*1: GBTCLK1_M2C_P/n can be assigned to reference clock of 4 MGT tiles by IC37.

For more details, please refer to “7.3.3 NGT reference clock selector”.

Table 7-9 HPC Column C & D Pin to FPGA Pin Assignment

Bank No.	Pin No.	C		D	Pin No.	Bank No.
		GND	1	*5 PG_C2M		
MGTTXP0_101	B9	DP0_C2M_P	2	GND		
MGTTXN0_101	A9	DP0_C2M_N	3	GND		
		GND	4	*1 GBTCLK0_M2C_P	*2	*2
		GND	5	*1 GBTCLK0_M2C_N	*2	*2
MGTRXP0_101	D10	DP0_M2C_P	6	GND		
MGTRXN0_101	C10	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	F19	0
		GND	9	LA01_N_CC	E19	0
0	G18	LA06_P	10	GND		
0	F18	LA06_N	11	LA05_P	F17	0
		GND	12	LA05_N	E17	0
		GND	13	GND		
0	F15	LA10_P	14	LA09_P	J14	0
0	E15	LA10_N	15	LA09_N	H14	0
		GND	16	GND		
		GND	17	LA13_P	G12	0
0	J13	LA14_P	18	LA13_N	F12	0
0	H13	LA14_N	19	GND		
		GND	20	LA17_P_CC	M15	0
		GND	21	LA17_N_CC	K15	0
0	L14	LA18_P_CC	22	GND		
0	K14	LA18_N_CC	23	LA23_P	H17	0
		GND	24	LA23_N	G17	0
		GND	25	GND		
0	K19	LA27_P	26	LA26_P	M18	0
0	J19	LA27_N	27	LA26_N	L18	0
		GND	28	GND		
		GND	29	TCK		
		*2 SCL	30	*4 TDI		
		*2 SDA	31	*4 TDO		
		GND	32	*6 3P3VAUX		
		GND	33	TMS		
		*3 GA0	34	TRST_L		
		*6 12P0V	35	*3 GA1		
		GND	36	*6 3P3V		
		*6 12P0V	37	GND		
		GND	38	*6 3P3V		
		*6 3P3V	39	GND		
		GND	40	*5 3P3V		

*2: GBTCLK0_M2C_P/n can be assigned to reference clock of 4 MGT tiles by IC37.

For more details, please refer to Figure 7-8 MGT reference clock structure

Table 7-10 HPC Column E & F Pin to FPGA Pin Assignment

Bank No.	Pin No.	E		F	Pin No.	Bank No.
		GND	1	*5 PG_M2C		
2	Y21	HA01_P_CC	2	GND		
2	AA21	HA01_N_CC	3	GND		
		GND	4	HA00_P_CC	W19	2
		GND	5	HA00_N_CC	Y19	2
2	Y17	HA05_P	6	GND		
2	AA17	HA05_N	7	HA04_P	Y16	2
		GND	8	HA04_N	AB16	2
2	AB17	HA09_P	9	GND		
2	AD17	HA09_N	10	HA08_P	AC15	2
		GND	11	HA08_N	AD15	2
2	AE15	HA13_P	12	GND		
2	AF15	HA13_N	13	HA12_P	AE17	2
		GND	14	HA12_N	AF17	2
2	AC19	HA16_P	15	GND		
2	AD19	HA16_N	16	HA15_P	AE21	2
		GND	17	HA15_N	AF21	2
2	AD22	HA20_P	18	GND		
2	AE22	HA20_N	19	HA19_P	AE23	2
		GND	20	HA19_N	AF23	2
2	AA11	HB03_P	21	GND		
2	AB11	HB03_N	22	HB02_P	AB10	2
		GND	23	HB02_N	AB9	2
2	AC9	HB05_P	24	GND		
2	AD9	HB05_N	25	HB04_P	AD8	2
		GND	26	HB04_N	AE8	2
2	AF7	HB09_P	27	GND		
2	AG7	HB09_N	28	HB08_P	AG6	2
		GND	29	HB08_N	AH6	2
2	AG8	HB13_P	30	GND		
2	AH8	HB13_N	31	HB12_P	AD10	2
		GND	32	HB12_N	AE10	2
2	AD12	HB19_P	33	GND		
2	AE12	HB19_N	34	HB16_P	AE13	2
		GND	35	HB16_N	AF13	2
2	AJ15	HB21_P	36	GND		
2	AK15	HB21_N	37	HB20_P	AC11	2
		GND	38	HB20_N	AD11	2
		*6 VADJ	39	GND		
		GND	40	*6 VADJ		

Table 7-11 HPC Column G & H Pin to FPGA Pin Assignment

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*7 VREF_A_M2C		
0	E16	CLK1_M2C_P	2	*5 PRSNT_M2C_L		
0	D16	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	B15	0
		GND	5	CLK0_M2C_N	A15	0
0	F21	LA00_P_CC	6	GND		
0	E21	LA00_N_CC	7	LA02_P	G20	0
		GND	8	LA02_N	F20	0
0	H19	LA03_P	9	GND		
0	G19	LA03_N	10	LA04_P	G22	0
		GND	11	LA04_N	F22	0
0	H16	LA08_P	12	GND		
0	G16	LA08_N	13	LA07_P	F23	0
		GND	14	LA07_N	E23	0
0	G14	LA12_P	15	GND		
0	F14	LA12_N	16	LA11_P	F13	0
		GND	17	LA11_N	E13	0
0	J12	LA16_P	18	GND		
0	H12	LA16_N	19	LA15_P	D24	0
		GND	20	LA15_N	C24	0
0	M13	LA20_P	21	GND		
0	L13	LA20_N	22	LA19_P	B25	0
		GND	23	LA19_N	A25	0
0	J18	LA22_P	24	GND		
0	H18	LA22_N	25	LA21_P	L17	0
		GND	26	LA21_N	K17	0
0	M19	LA25_P	27	GND		
0	L19	LA25_N	28	LA24_P	M20	0
		GND	29	LA24_N	L20	0
0	L21	LA29_P	30	GND		
0	K21	LA29_N	31	LA28_P	K20	0
		GND	32	LA28_N	J20	0
0	J22	LA31_P	33	GND		
0	H22	LA31_N	34	LA30_P	H21	0
		GND	35	LA30_N	G21	0
0	F24	LA33_P	36	GND		
0	E24	LA33_N	37	LA32_P	E25	0
		GND	38	LA32_N	D25	0
		*6 VADJ	39	GND		
		GND	40	*6 VADJ		

Table 7-12 HPC Column J & K Pin to FPGA Pin Assignment

Bank No.	Pin No.	J		K	Pin No.	Bank No.
		GND	1	*7 VREF_B_M2C		
2	AF16	CLK3_M2C_P	2	GND		
2	AG16	CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P	AC16	2
		GND	5	CLK2_M2C_N	AD16	2
2	AB21	HA03_P	6	GND		
2	AC21	HA03_N	7	HA02_P	W20	2
		GND	8	HA02_N	Y20	2
2	AA19	HA07_P	9	GND		
2	AB19	HA07_N	10	HA06_P	AA18	2
		GND	11	HA06_N	AB18	2
2	AD18	HA11_P	12	GND		
2	AE18	HA11_N	13	HA10_P	AA22	2
		GND	14	HA10_N	AC22	2
2	AE19	HA14_P	15	GND		
2	AF19	HA14_N	16	HA17_P_CC	AD20	2
		GND	17	HA17_N_CC	AE20	2
2	AE24	HA18_P	18	GND		
2	AF24	HA18_N	19	HA21_P	AC24	2
		GND	20	HA21_N	AD24	2
2	AB20	HA22_P	21	GND		
2	AC20	HA22_N	22	HA23_P	AB23	2
		GND	23	HA23_N	AC23	2
2	AB12	HB01_P	24	GND		
2	AC12	HB01_N	25	HB00_P_CC	W12	2
		GND	26	HB00_N_CC	Y12	2
2	AE9	HB07_P	27	GND		
2	AF9	HB07_N	28	HB06_P_CC	Y14	2
		GND	29	HB06_N_CC	AA14	2
2	AH7	HB11_P	30	GND		
2	AK7	HB11_N	31	HB10_P	W14	2
		GND	32	HB10_N	Y13	2
2	AE11	HB15_P	33	GND		
2	AF11	HB15_N	34	HB14_P	AB13	2
		GND	35	HB14_N	AC13	2
2	AD14	HB18_P	36	GND		
2	AE14	HB18_N	37	HB17_P_CC	AB14	2
		GND	38	HB17_N_CC	AC14	2
		*8 VIO_B_M2C	39	GND		
		GND	40	*8 VIO_B_M2C		

*** 1 GBTCLK0_M2C_P,N**

This signal is used for reference clock of MGT.

*** 2 SCL,SDA**

The board provides test points TP32 and TP33 (with pullup resistors pad) to enable I^2C communications with the FPGA mezzanine card.

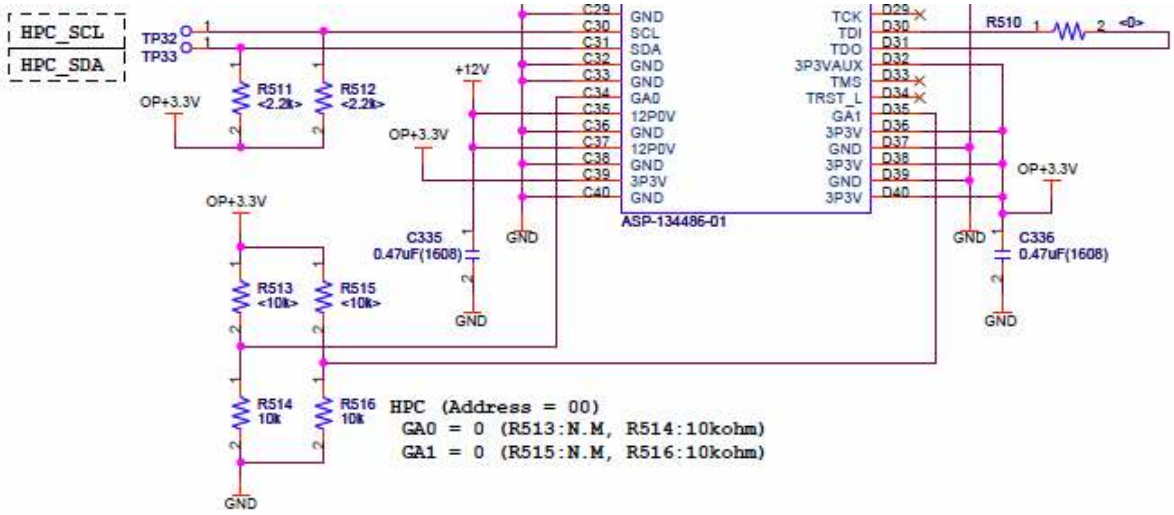


Figure 7-14 SDA, SCL, GA1/0 TDI/TDO

*** 3 GA[1:0]**

The board has the above circuit design for notification of an ID to the FPGA mezzanine card. By default, the value is set to 00.

*** 4 TDI,TDO**

The board provides a loopback structure for JTAG communication from the FPGA mezzanine card. By default, this loopback function is not provided because the R510 resistor is not installed.

*** 5 PG_C2M, PG_M2C, PRSNT_M2C_L**

The board provides a structure to output to the FPGA mezzanine card. It also provides a similar structure for the column of F and H pins of the FMC connector. By default, it is set to open. The PG_M2C, PRSNT_M2C_L also has a similar structure.

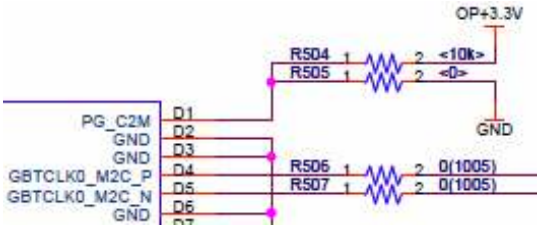


Figure 7-15 PG_C2M, PG_M2C,PRSNT_M2C_L

Table 7-13 PG_C2M, PRSNT_M2C_L settings

Pin No.	Signal	Level settings	
		H	L
D1	PG_C2M	R504	R505
F1	PG_M2C	R517	R518
H2	PRSNT_M2C_L	R523	R524

*** 6 Power Supply**

The board provides a 12V output to the 12P0V pin and a 3.3V output to the 3P3V and 3P3VAUX pins. 3.3V and 2.5V output are also selectable for VADJ pins as shown in the following circuit diagram. The target FPGA pins are E39, F40, G39 and H40. The HPC_VADJ voltage supply is set by jumping across the identical pins on jumpers JP8 and JP9. The power status can be monitored by the adjacent LED.

Caution:

Do not jumper more than two portions of JP8 and JP9.

Always jumper the same pins of both JP8 and JP9.

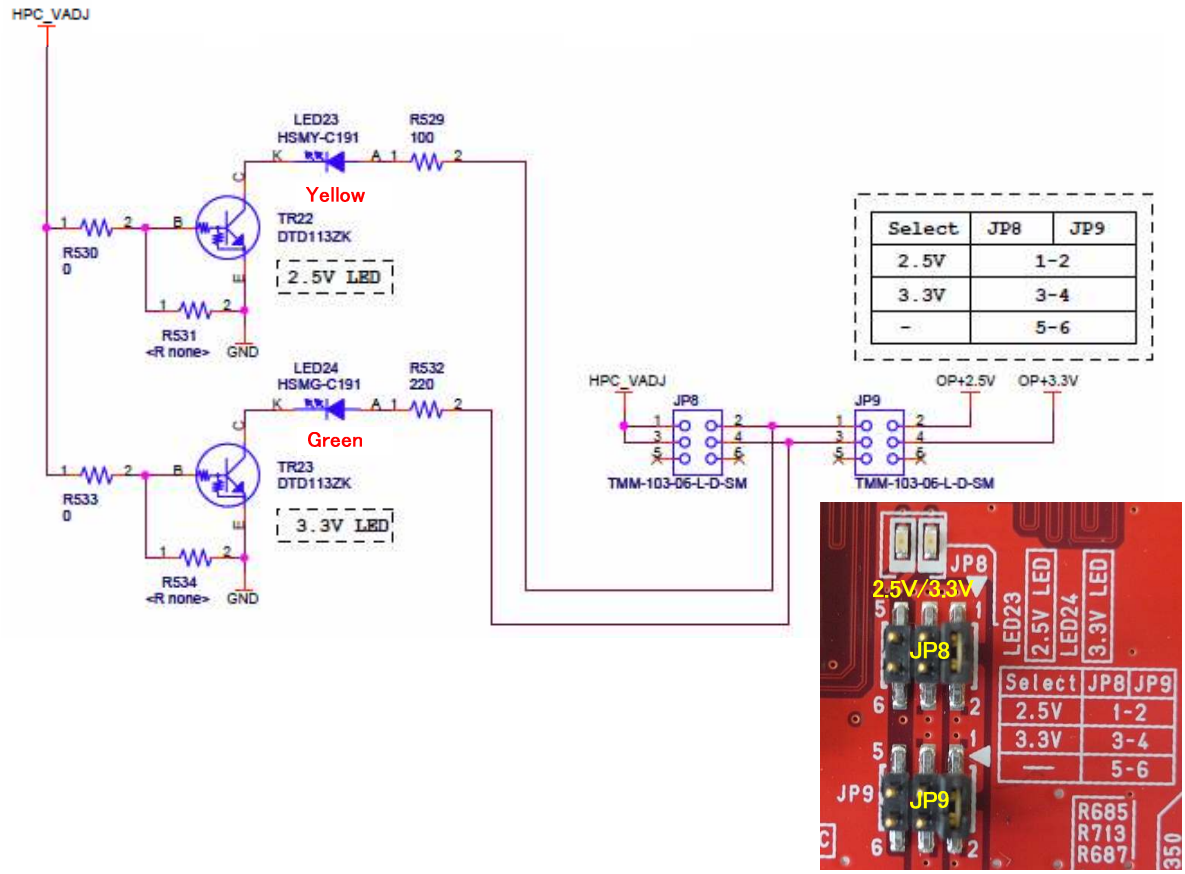


Figure 7-16 VADJ

***7 VREF_A_M2C,VREF_B_M2C**

The VREF_A_M2C terminal of the H1 pin can be monitored by TP36 and the VREF_B_M2C terminal of the K1 pin by TP34.

***8 VIO_B_M2C**

The VIO_B_M2C terminal of each J39 and K40 pin can be monitored by TP35.

7.4.2. LPC(Low-Pin Count) LPC1

The FMC low-pin count connector connects the following number of signals:

Low Speed: LA 34 pair (68 single-end) and 2 clocks.

FPGA IO Bank3 cannot output LVDS signals. It is a limitation of the FPGA.

Table 7-14 LPC1 (CN3) Column C & D Pin to FPGA Pin assignment

Bank	Pin No.	C		D	Pin No.	Bank No.
		GND	1	*4 PG_C2M		
		DP0_C2M_P	2	GND		
		DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P		
		GND	5	GBTCLK0_M2C_N		
		DP0_M2C_P	6	GND		
		DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	M10	0
		GND	9	LA01_N_CC	L10	0
0	L11	LA06_P	10	GND		
0	K11	LA06_N	11	LA05_P	K10	0
		GND	12	LA05_N	J10	0
		GND	13	GND		
0	F11	LA10_P	14	LA09_P	G10	0
0	E11	LA10_N	15	LA09_N	F10	0
		GND	16	GND		
		GND	17	LA13_P	D8	0
0	B7	LA14_P	18	LA13_N	C8	0
0	A7	LA14_N	19	GND		
		GND	20	LA17_P_CC	H11	0
		GND	21	LA17_N_CC	G11	0
0	H7	LA18_P_CC	22	GND		
0	G7	LA18_N_CC	23	LA23_P	F8	0
		GND	24	LA23_N	E8	0
		GND	25	GND		
0	D6	LA27_P	26	LA26_P	E7	0
0	C6	LA27_N	27	LA26_N	D7	0
		GND	28	GND		
		GND	29	TCK		
		*1 SCL	30	*3 TDI		
		*1 SDA	31	*3 TDO		
		GND	32	*6 3P3VAUX		
		GND	33	TMS		
		*2 GA0	34	TRST_L		
		*6 12P0V	35	*2 GA1		
		GND	36	*6 3P3V		
		*6 12P0V	37	GND		
		GND	38	*6 3P3V		
		*6 3P3V	39	GND		
		GND	40	*6 3P3V		

Table 7-15 LPC1 (CN3) Column G & H pin Pin to FPGA Pin assignment

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*5 VREF_A_M2C		
0	H15	CLK1_M2C_P	2	*4 PRSNT_M2C_L		
0	G15	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	V4	3
		GND	5	CLK0_M2C_N	V3	3
0	F6	LA00_P_CC	6	GND		
0	E6	LA00_N_CC	7	LA02_P	U5	3
		GND	8	LA02_N	U4	3
0	J8	LA03_P	9	GND		
0	H8	LA03_N	10	LA04_P	U7	3
		GND	11	LA04_N	U6	3
0	L12	LA08_P	12	GND		
0	K12	LA08_N	13	LA07_P	N8	3
		GND	14	LA07_N	N7	3
0	F9	LA12_P	15	GND		
0	E9	LA12_N	16	LA11_P	M7	3
		GND	17	LA11_N	M6	3
0	B6	LA16_P	18	GND		
0	A6	LA16_N	19	LA15_P	T4	3
		GND	20	LA15_N	T3	3
3	V2	LA20_P	21	GND		
3	V1	LA20_N	22	LA19_P	T7	3
		GND	23	LA19_N	T6	3
3	R7	LA22_P	24	GND		
3	R6	LA22_N	25	LA21_P	P7	3
		GND	26	LA21_N	P6	3
3	R5	LA25_P	27	GND		
3	R4	LA25_N	28	LA24_P	N5	3
		GND	29	LA24_N	N4	3
3	P4	LA29_P	30	GND		
3	P3	LA29_N	31	LA28_P	N3	3
		GND	32	LA28_N	N	3
3	P2	LA31_P	33	GND		
3	P1	LA31_N	34	LA30_P	R	3
		GND	35	LA30_N	R1	3
3	T2	LA33_P	36	GND		
3	T1	LA33_N	37	LA32_P	U3	3
		GND	38	LA32_N	U1	3
		*6 VADJ	39	GND		
		GND	40	*6 VADJ		

*** 1 SCL,SDA**

The board provides test points TP27 and TP28 (with pullup resistors pad) to enable I^2C communications with the LPC1 (CN3) FPGA mezzanine card.

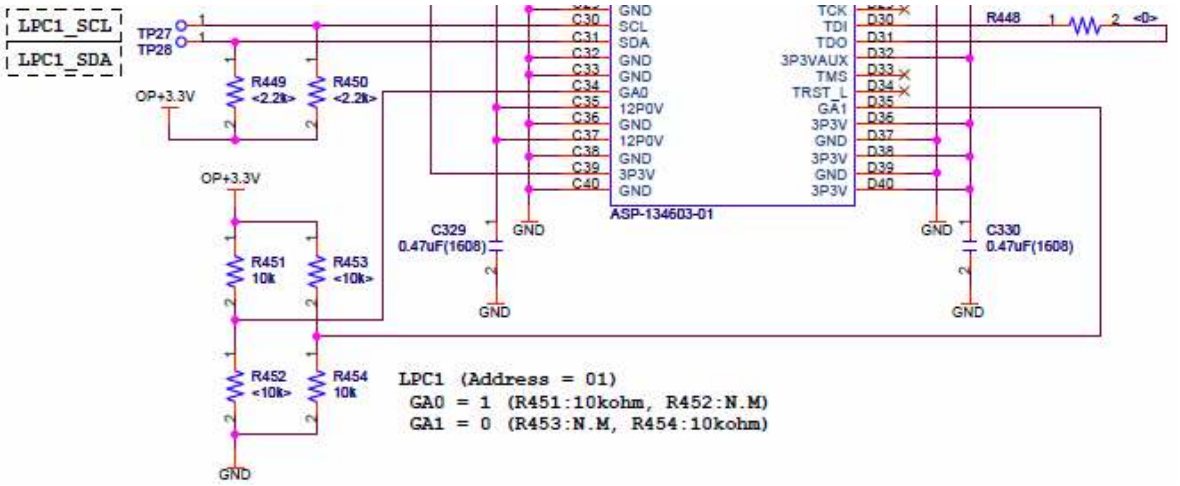


Figure 7-17 SDA,SCL,GA1/0 TDI/TD0

*** 2 GA[1:0]**

The board has the above circuit design for notification of an ID to the FPGA mezzanine card. By default, the value is set to 01.

*** 3 TDI,TDO**

The board provides a loopback structure for JTAG communication from the FPGA mezzanine card. By default, this loopback function is not provided because the R448 resistor is not installed.

*** 4 PG_C2M, PRSNT_M2C_L**

The board provides a structure to output to the FPGA mezzanine card. By default, it is set to open.

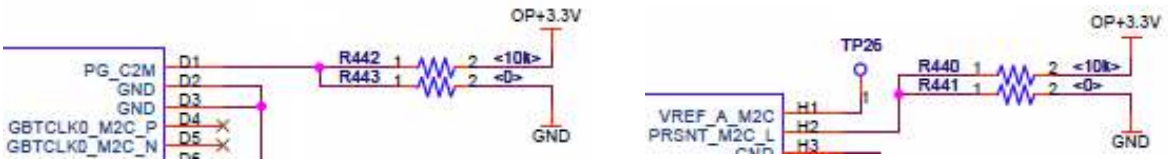


Figure 7-18 PG_C2M,PRSNT_M2C_L

Table 7-16 PG_C2M, PRSNT_M2C_L settings

Pin No.	Signal	Level settings	
		H	L
D1	PG_C2M	R442	R443
H2	PRSNT_M2C_L	R440	R441

***5 VREF_A_M2C**

The board provides a test pad (TP26) to monitor the H1 pin (VREF_A_M2C) of the FMC connector.

***6 Power Supply**

The board provides a 12V output to the 12P0V pin and a 3.3V output to the 3P3V and 3P3VAUX pins. 3.3V and 2.5V output are also selectable for VADJ pins as shown in the following circuit diagram. The LPC1_VADJ voltage supply is set by jumping across the identical pins on jumpers JP4 and JP5. The power status can be monitored by the adjacent LED.

Caution:

Do not jumper more than two portions of JP4 and JP5.

Always jumper the same portion of JP4 and JP5.

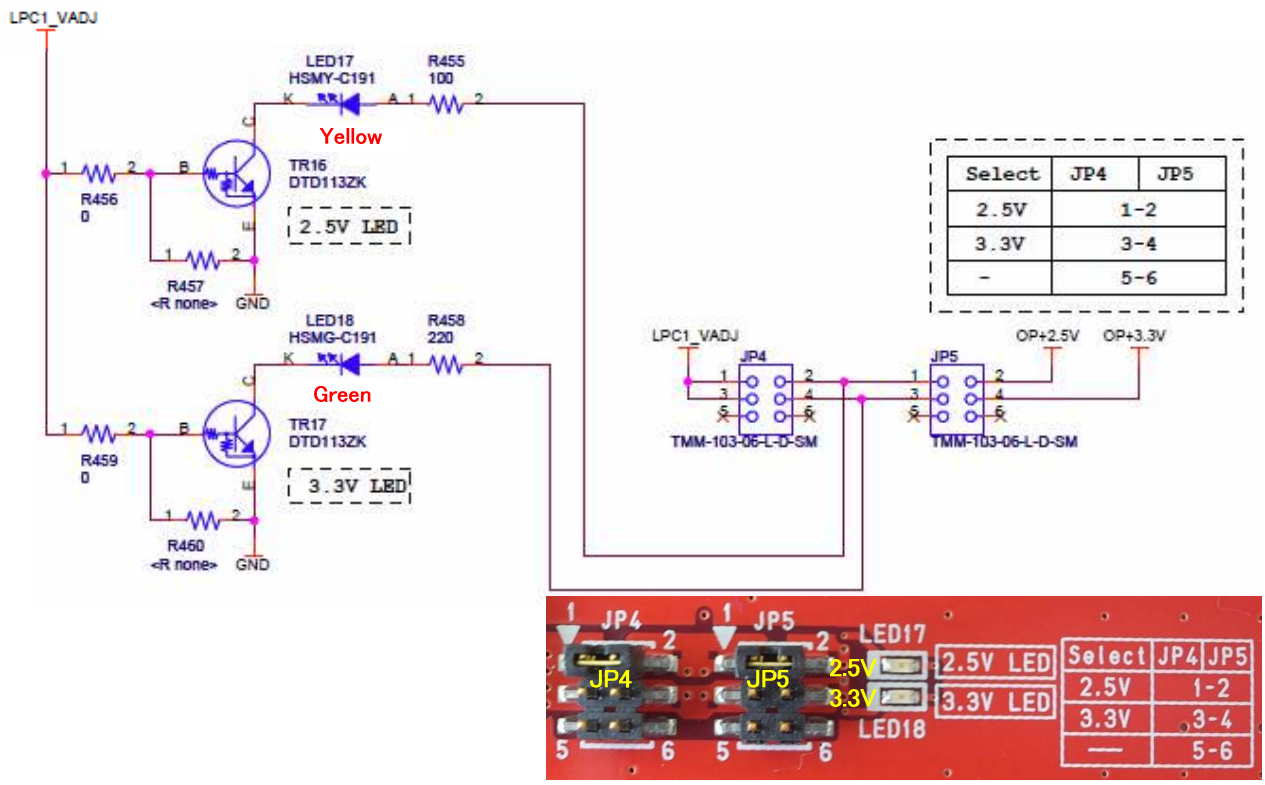


Figure 7-19 VADJ

7.4.3. LPC (Low-Pin Count) LPC2

The FMC low-pin count connector connects the following number of signals:

Low Speed: LA 34 pair(68 single-end) and 2 clocks.

FPGA IO Bank3 cannot output LVDS signals. It is a limitation of FPGA.

Table 7-17 LPC2 (CN4) Column C & D Pin to FPGA Pin Assignment

Bank No.	Pin No.	C		D	Pin No.	Bank No.
		GND	1	*4 PG_C2M		
		DP0_C2M_P	2	GND		
		DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P		
		GND	5	GBTCLK0_M2C_N		
		DP0_M2C_P	6	GND		
		DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	W10	3
		GND	9	LA01_N_CC	W9	3
3	AE4	LA06_P	10	GND		
3	AF4	LA06_N	11	LA05_P	AE5	3
		GND	12	LA05_N	AG5	3
		GND	13	GND		
3	AJ4	LA10_P	14	LA09_P	AH3	3
3	AK4	LA10_N	15	LA09_N	AK3	3
		GND	16	GND		
		GND	17	LA13_P	AD7	3
3	Y9	LA14_P	18	LA13_N	AE7	3
3	Y8	LA14_N	19	GND		
		GND	20	LA17_P_CC	Y2	3
		GND	21	LA17_N_CC	Y1	3
3	AB4	LA18_P_CC	22	GND		
3	AB3	LA18_N_CC	23	LA23_P	AC3	3
		GND	24	LA23_N	AC1	3
		GND	25	GND		
3	AF1	LA27_P	26	LA26_P	AE3	3
3	AG1	LA27_N	27	LA26_N	AE1	3
		GND	28	GND		
		GND	29	TCK		
		*1 SCL	30	*3 TDI		
		*1 SDA	31	*3 TDO		
		GND	32	*6 3P3VAUX		
		GND	33	TMS		
		*2 GA0	34	TRST_L		
		*6 12P0V	35	*2 GA1		
		GND	36	*6 3P3V		
		*6 12P0V	37	GND		
		GND	38	*6 3P3V		
		*6 3P3V	39	GND		
		GND	40	*6 3P3V		

Table 7-18 LPC2 (CN4) Column G & H Pin to FPGA Pin Assignment

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*5 VREF_A_M2C		
3	AB2	CLK1_M2C_P	2	*4 PRSNT_M2C_L		
3	AB1	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	AA3	3
		GND	5	CLK0_M2C_N	AA1	3
3	Y7	LA00_P_CC	6	GND		
3	Y6	LA00_N_CC	7	LA02_P	W7	3
		GND	8	LA02_N	W6	3
3	AA7	LA03_P	9	GND		
3	AA6	LA03_N	10	LA04_P	AB7	3
		GND	11	LA04_N	AB6	3
3	AC6	LA08_P	12	GND		
3	AD6	LA08_N	13	LA07_P	AJ2	3
		GND	14	LA07_N	AK2	3
3	AH5	LA12_P	15	GND		
3	AK5	LA12_N	16	LA11_P	AE6	3
		GND	17	LA11_N	AF6	3
3	AA10	LA16_P	18	GND		
3	AA9	LA16_N	19	LA15_P	W11	3
		GND	20	LA15_N	Y11	3
3	W3	LA20_P	21	GND		
3	W1	LA20_N	22	LA19_P	Y4	3
		GND	23	LA19_N	Y3	3
3	AD2	LA22_P	24	GND		
3	AD1	LA22_N	25	LA21_P	AH1	3
		GND	26	LA21_N	AJ1	3
3	AF3	LA25_P	27	GND		
3	AG3	LA25_N	28	LA24_P	AG4	3
		GND	29	LA24_N	AH4	3
3	AF2	LA29_P	30	GND		
3	AH2	LA29_N	31	LA28_P	AD4	3
		GND	32	LA28_N	AD3	3
3	AC5	LA31_P	33	GND		
3	AC4	LA31_N	34	LA30_P	AA5	3
		GND	35	LA30_N	AA4	3
3	V8	LA33_P	36	GND		
3	V7	LA33_N	37	LA32_P	V10	3
		GND	38	LA32_N	V9	3
		*6 VADJ	39	GND		
		GND	40	*6 VADJ		

*** 1 SCL,SDA**

The board provides test points TP30 and TP31 (with pullup resistors pad) to enable I^2C communications with the FPGA mezzanine card

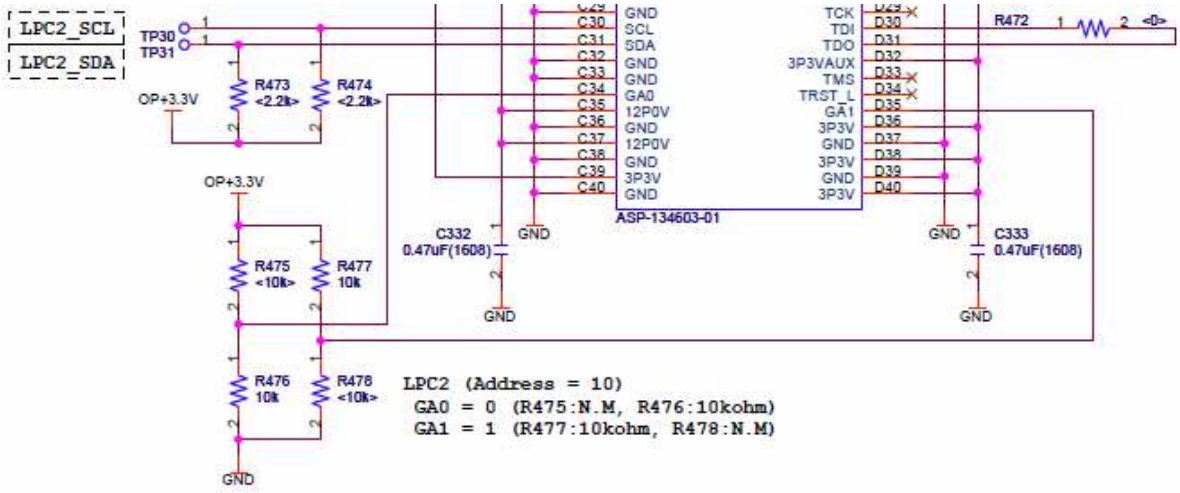


Figure 7-20 SDA,SCL,GA1/0 TDI/TD0

*** 2 GA[1:0]**

The board has the above circuit design for notification of an ID to the FPGA mezzanine card. By default, the value is set to 10.

*** 3 TDI,TDO**

The board provides a loopback structure for JTAG communication from the FPGA mezzanine card. By default, this loopback function is not provided because the R472 resistor is not installed.

*** 4 PG_C2M, PRSNT_M2C_L**

The board provides a structure to output to the FPGA mezzanine card. By default, it is set to open.

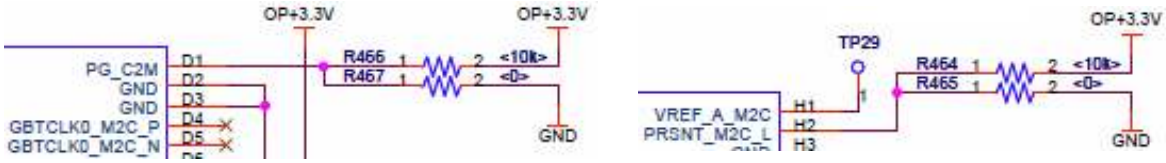


Figure 7-21 PG_C2M,PRSNT_M2C_L

Table 7-19 PG_C2M, PRSNT_M2C_L settigs

Pin No.	Signal	Settings	
		H	L
D1	PG_C2M	R466	R467
H2	PRSNT_M2C_L	R464	R465

*** 5 VREF_A_M2C**

The board provides a test pad (TP29) to monitor the H1 pin (VREF_A_M2C) of the FMC connector.

*** 6 Power Supply**

The board provides a 12V output to the 12P0V pin and a 3.3V output to the 3P3V and 3P3VAUX pins. 3.3V and 2.5V output are also selectable for VADJ pins as shown in the following circuit diagram. The LPC2_VADJ voltage supply is set by jumping across the identical pins on jumpers JP6 and JP7. The power status can be monitored by the adjacent LED.

Caution:

Do not jumper more than two portions of JP6 and JP7.

Always jumper the same portion of JP6 and JP7.

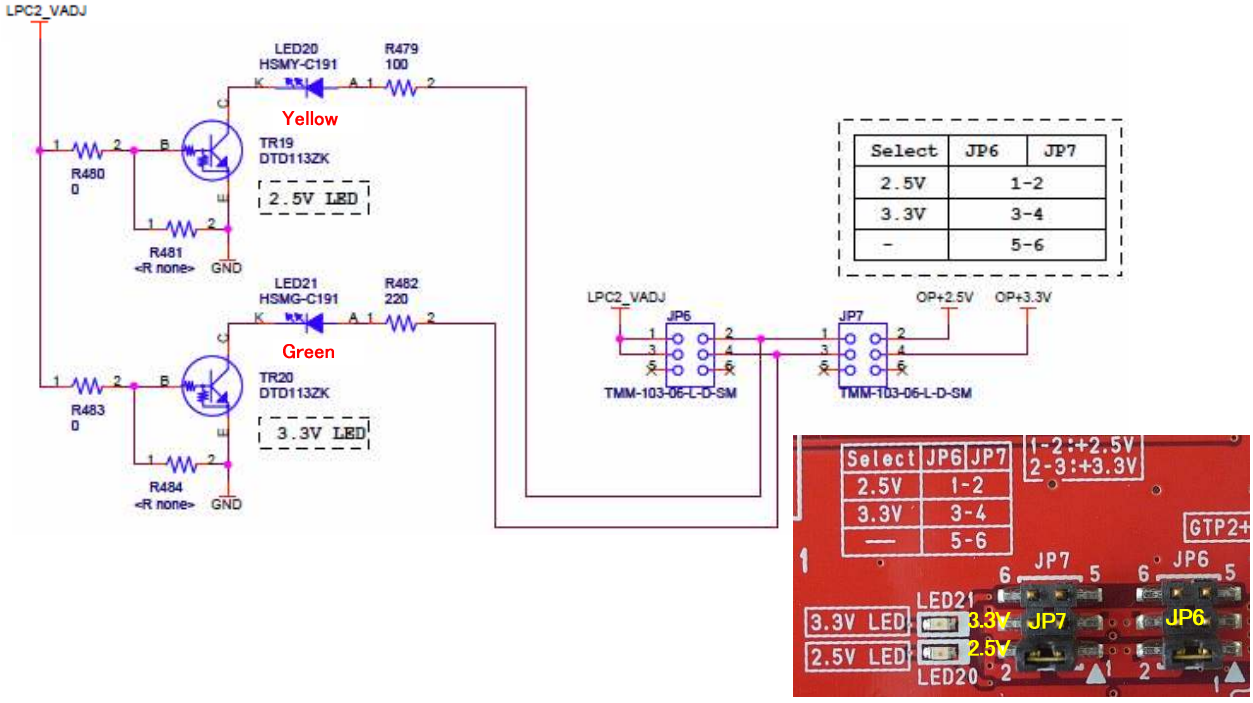


Figure 7-22 VADJ

7.5. DDR3 SDRAM

The board provides three independent, 1 Gbit Micron DDR3 SDRAMs (MT41J64M16LA-15E)

The following pins are connected:

A[12:0], DQU[7:0], DQL[7:0],ODT, DQSU, /DQSU, DQSL, /DQSL, DMU, DML, CK, /CK, CKE, /RAS, /CAS, /WE, BA[2:0], /RESET

/CS is hardwired low

A[14], A[13] are memory address expansion bits.

The board addresses 1 Gb using A[12:0].

Specifications

1Gbit (8Mword x 16bit x 8bank), 1066 (7-7-7) (Please refer to the Micron data sheet.)

Address Structure

Bank =3bit

Address = 13bit (Row address = 13bit / Column address = 10bit)

Data Bus Structure

Each byte data strobe with write and read DQS

Each byte data mask (DM)

Figure 7-23 DDR3 SDRAM

Table 7-20 DDR3 SDRAM pin assignment

DDR3 Pin Name	Bank1 (IC27)	Bank4 (IC28)	Bank5 (IC23)
A0	U29	D4	D28
A1	U30	D3	D30
A2	T27	A3	C30
A3	V28	E5	E29
A4	R30	C5	F27
A5	V26	F2	H26
A6	V27	F1	H27
A7	T26	B3	C29
A8	P26	B2	B27
A9	P27	A2	A27
A10	R29	D5	F26
A11	N28	G4	A26
A12	P30	A4	B30
A13	N29	B5	A28
A14	N30	A5	A29
BA0	T28	D2	D27
BA1	T30	D1	C27
BA2	R28	F3	D26
CK	U27	E3	E27
CKN	U28	E1	E28
RASN	W27	C1	K26
CASN	W28	B1	K27
CKE	P28	C4	B29
WE	R27	F4	E26
ODT	V30	E4	E30

DDR3 Pin Name	Bank1 (IC27)	Bank4 (IC28)	Bank5 (IC23)
DQL0	Y26	H4	H28
DQL1	Y27	H3	H30
DQL2	AA27	J3	G29
DQL3	AA28	J1	G30
DQL4	W29	G3	G27
DQL5	W30	G1	G28
DQL6	Y28	H2	F28
DQL7	Y30	H1	F30
DQU0	AD28	M4	L27
DQU1	AD30	M3	L28
DQU2	AC27	L5	L29
DQU3	AC28	L4	L30
DQU4	AE29	L3	M26
DQU5	AE30	L1	M27
DQU6	AE27	M2	M28
DQU7	AE28	M1	M30
DQSL	AA29	J5	J29
DQSLN	AA30	J4	J30
DQSU	AC29	K2	K28
DQSUN	AC30	K1	K30
DML	AB30	K3	J28
DMU	AB28	K4	J27
RESETN	N27	G5	C26
RZQ	M23	L7	G25
ZIO	W24	J6	N24

Notice: Please refer to Xilinx answer record #34055 "*MIG Spartan-6 FPGA MCB - What are the requirements for the RZQ and ZIO pins?*" for information on how to use the peculiar signals RZQ/ZIO of the Memory Controller Block (MCB). The default setting of RZQ is 100 Ohm pull-down and /ZIO is N.C.

7.6. USB (UART)

The board provides a MiniUSB B-Type interface connector (CN13) as a means to communicate between a computer terminal emulator (using the USB-RS232C conversion device (IC40) for bidirectional UART based communication) and the FPGA.

JP10 enables the SCL pin of the USB-RS232C conversion device's associated EEPROM. SW13 is the reset push button for IC40.

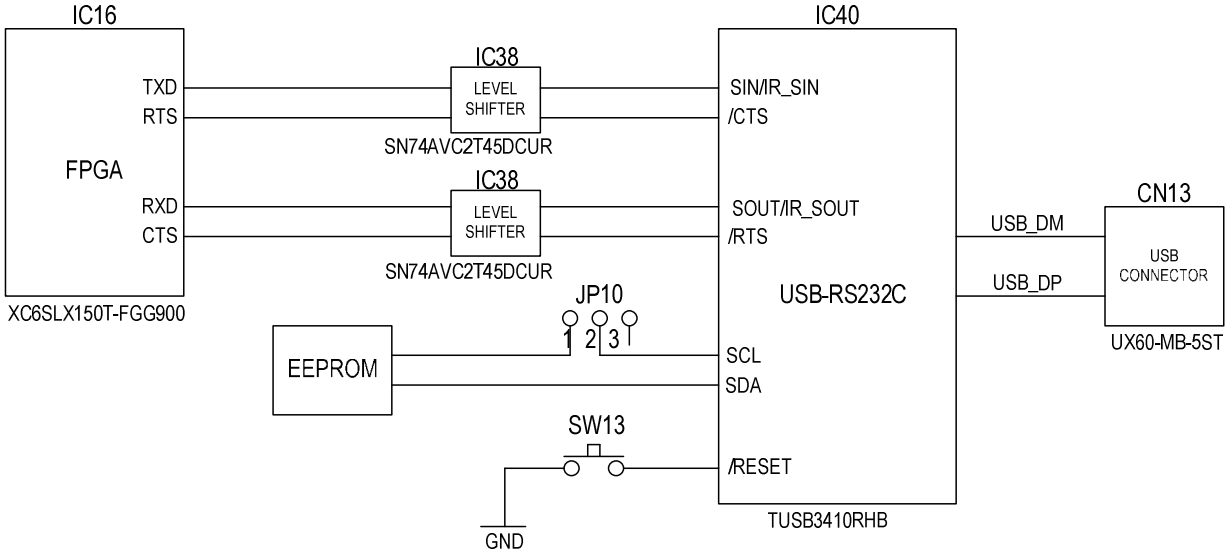


Figure 7-24 USB (UART)

Table 7-21 UART pin assignment

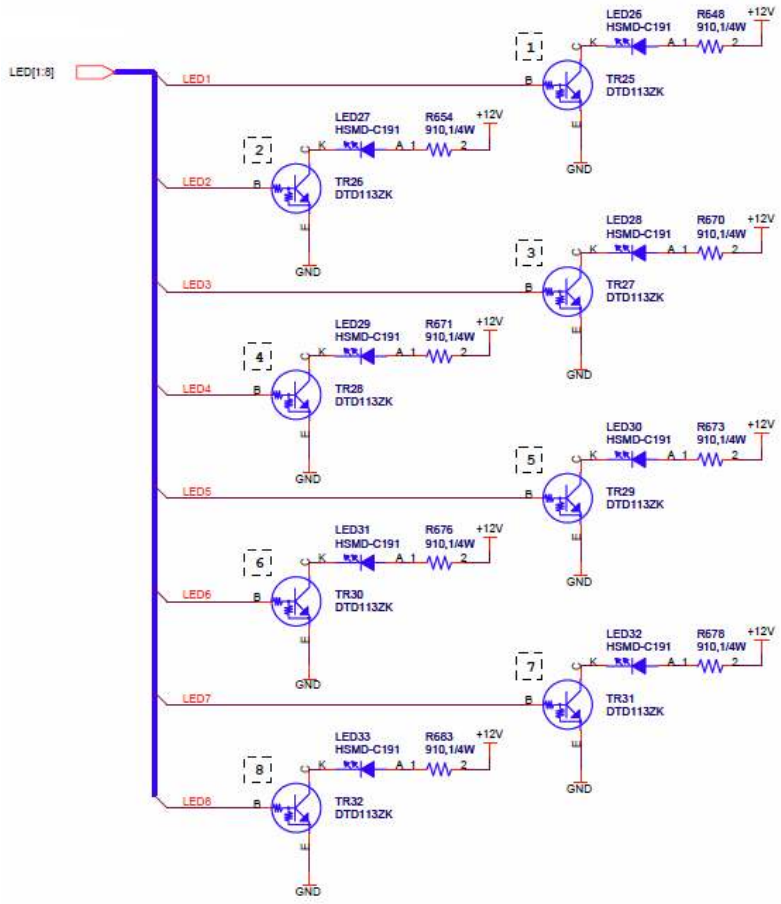
Pin No.	Signal Name	Bank	Level
Y25	FP_RXD	1	1.5V
AG26	FP_TXD	1	
AH26	FP_CTS	1	
AA25	FP_RTS	1	

Table 7-22 Serial EEPROM SCL

JP10	connection
1-2 Short	Connected
2-3 Short	Un connected

7.7. LED

The board provides 8 onboard LEDs. These LEDs will light when the corresponding FPGA output pin is driven high.



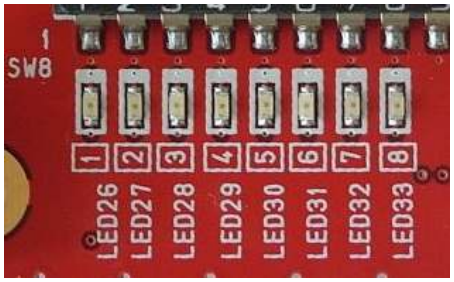


Figure 7-25 LED

Table 7-23 LED pin assignment

Device		FPGA		
Name	Signal Name	Pin No.	Bank	Level
LED26	LED1	R21	1	1.5V
LED27	LED2	R22	1	
LED28	LED3	AF28	1	
LED29	LED4	AF30	1	
LED30	LED5	P22	1	
LED31	LED6	P23	1	
LED32	LED7	AG29	1	
LED33	LED8	AG30	1	

7.8. DIP Switch

The board provides a 10 pole DIP switch. When a DIP switch is set to the ON side, it generates a high input to the associated FPGA pin.

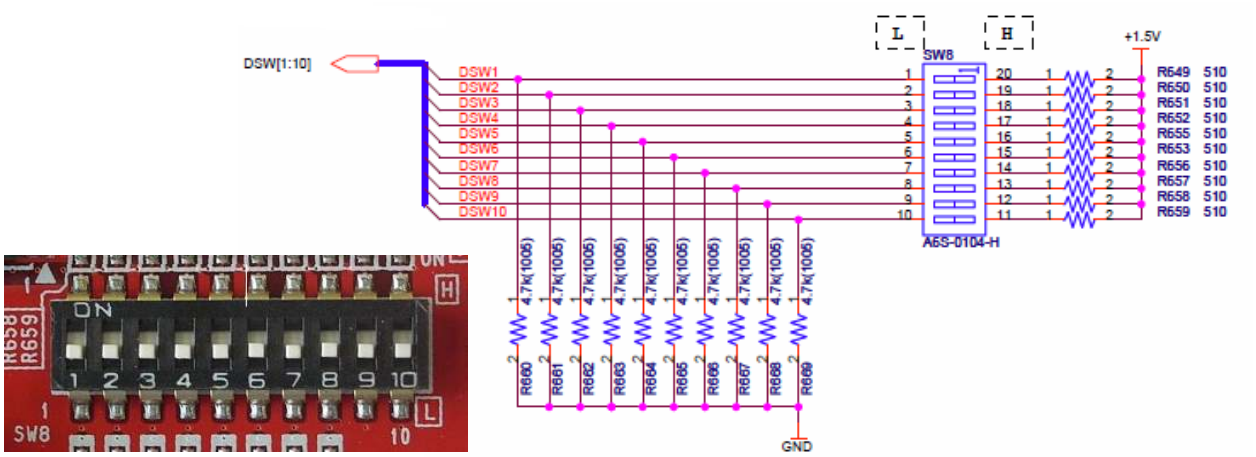


Figure 7-26 DIP Switch Diagram and Location

Table 7-24 DIP Switch Pin Assignment

Device		FPGA		
Name	Signal Name	Pin No.	Bank	Level
SW8	DSW1	P24	1	1.5V
	DSW2	P25	1	
	DSW3	AH30	1	
	DSW4	AJ30	1	
	DSW5	R24	1	
	DSW6	R25	1	
	DSW7	AJ29	1	
	DSW8	AK29	1	
	DSW9	T24	1	
	DSW10	T25	1	

7.9. Push Button Switches

The board provides 4 push button switches. When a switch is depressed, it generates a high input to the associated FPGA pin.

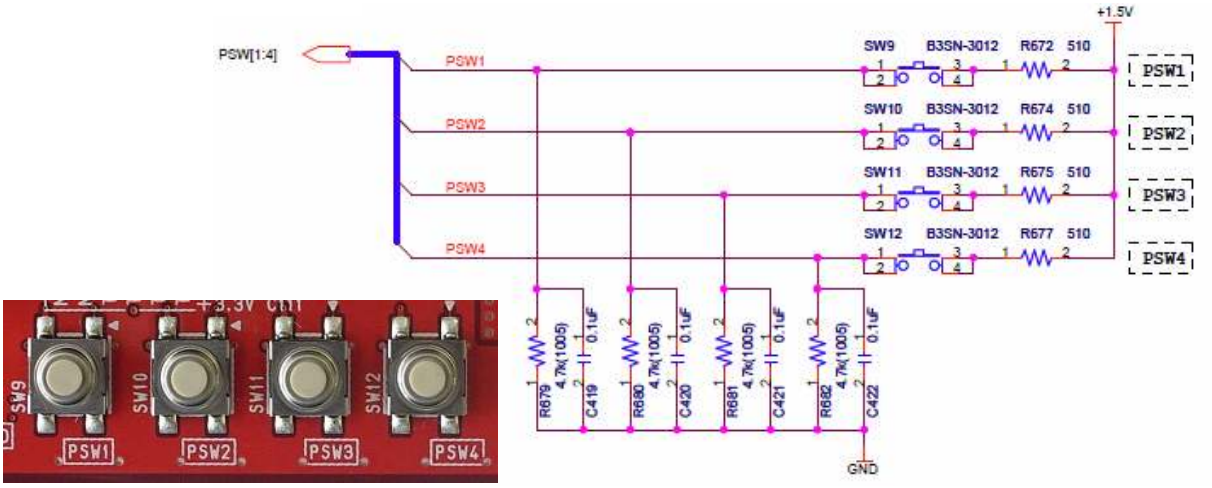


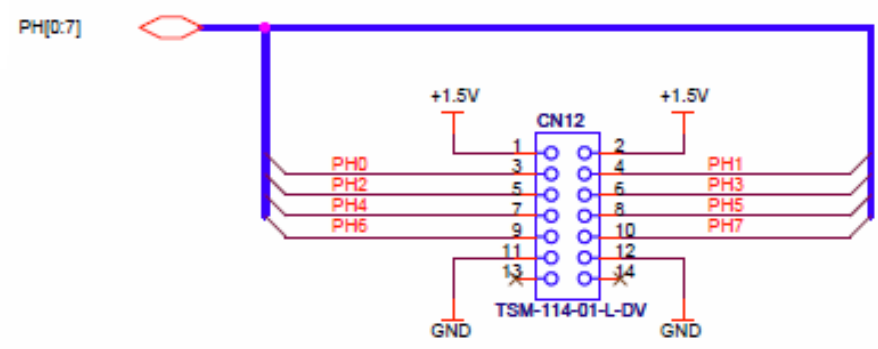
Figure 7-27 Push Button Switch

Table 7-25 Push Button Switch Pin Assignment

Device		FPGA		
Name	Signal Name	Pin No.	Bank	Level
SW9	PSW1	AJ28	1	1.5V
SW10	PSW2	AK28	1	
SW11	PSW3	U24	1	
SW12	PSW4	U25	1	

7.10. Pin Header

The board provides a 14 header connector (CN12). 8 pins are connected to the FPGA. Interface level is 1.5V.



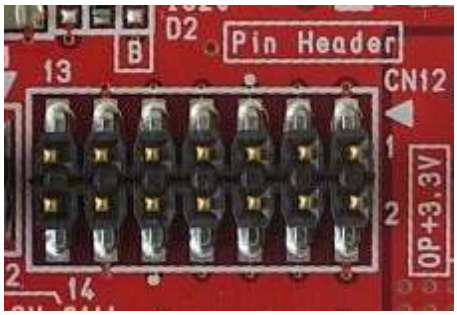


Figure 7-28 PinHeader

Table 7-26 Pin Header pin assignment

FPGA		Pin Header				FPGA	
Bank No.	Pin No.	Signal Name	Pin No.		Signal Name	Pin No.	Bank No.
-	-	1.5V	1	2	1.5V	-	-
1	AG27	PH0	3	4	PH1	AG28	1
1	V23	PH2	5	6	PH3	V24	1
1	AD26	PH4	7	8	PH5	AD27	1
1	W21	PH6	9	10	PH7	W22	1
-	-	GND	11	12	GND	-	-
-	-	-	13	14	-	-	-

7.11. Battery

A Battery socket is not mounted on the solder side of the board at location CN2

Battery power is connected to VBATT (AB26) of FPGA. Please use “CR1220” size battery.

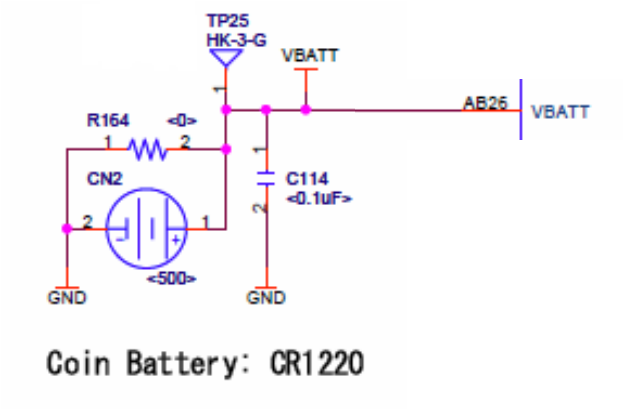


Figure 7-29 Battery

8. Appendix

8.1. Creating a Configuration File

This section describes how to create a configuration file using Xilinx ISE software version 12.2

Create a configuration file to write into the Flash memory.

1. Double-click **Generate Target PROM/ACE File**.

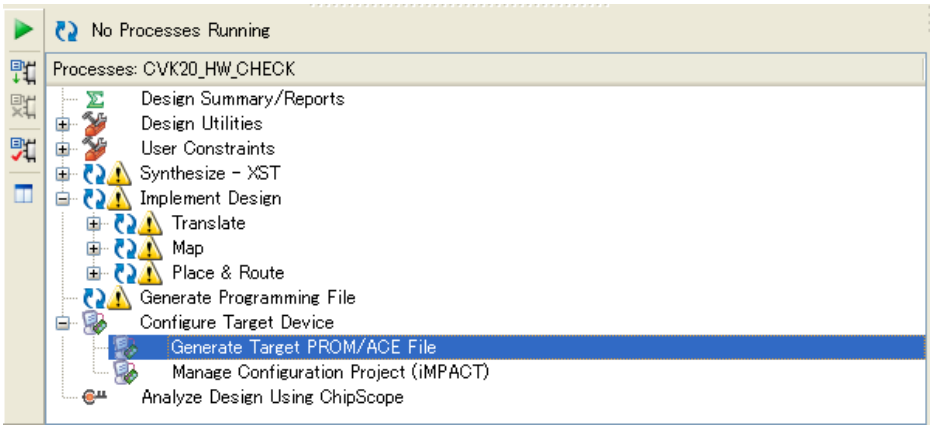


Figure 8-1 Creating a Configuration File with ISE 12.2

2. Double-click **Create PROM File**.

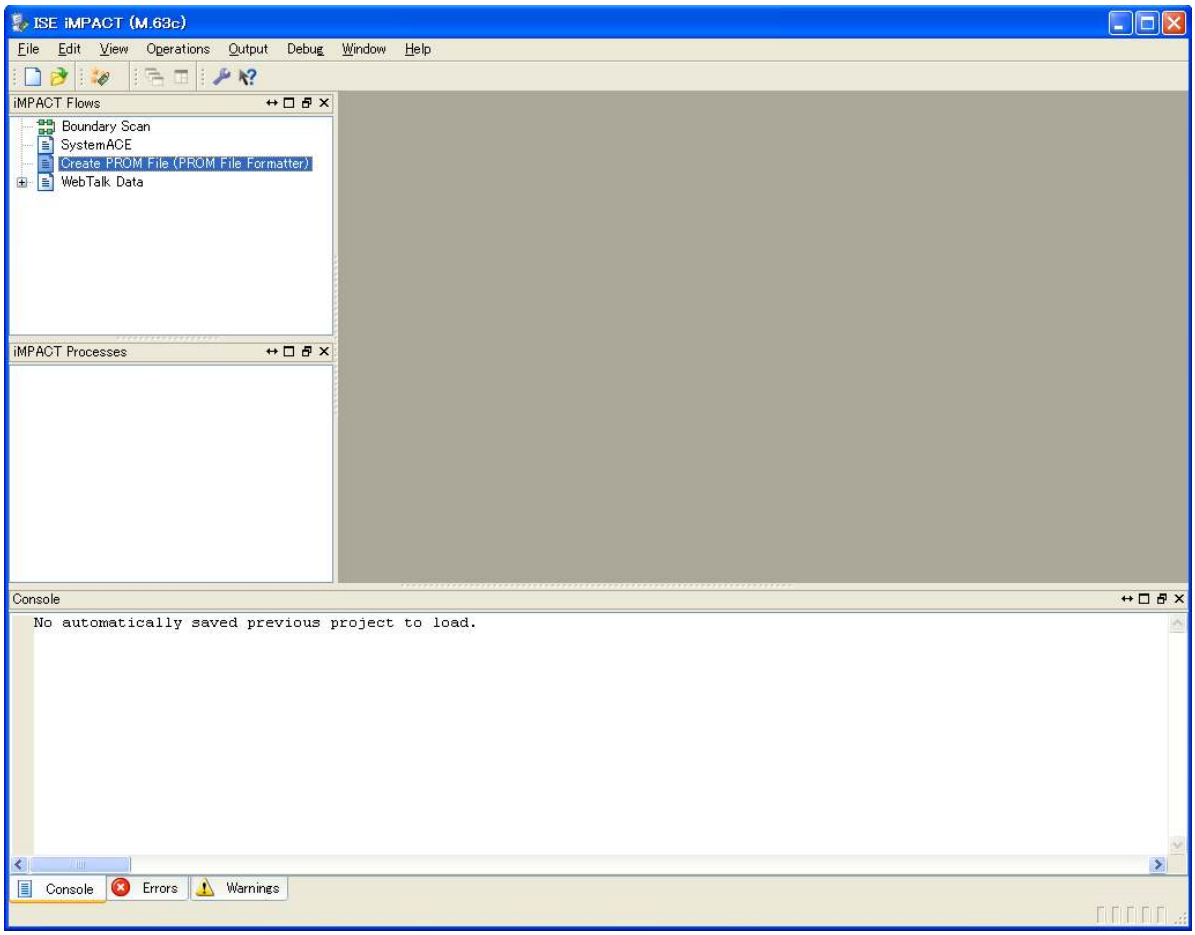


Figure 8-2 iMPACT Window 1

3. Choose **SPI Flash - Configure Single FPGA** and then click the right-pointing arrow.

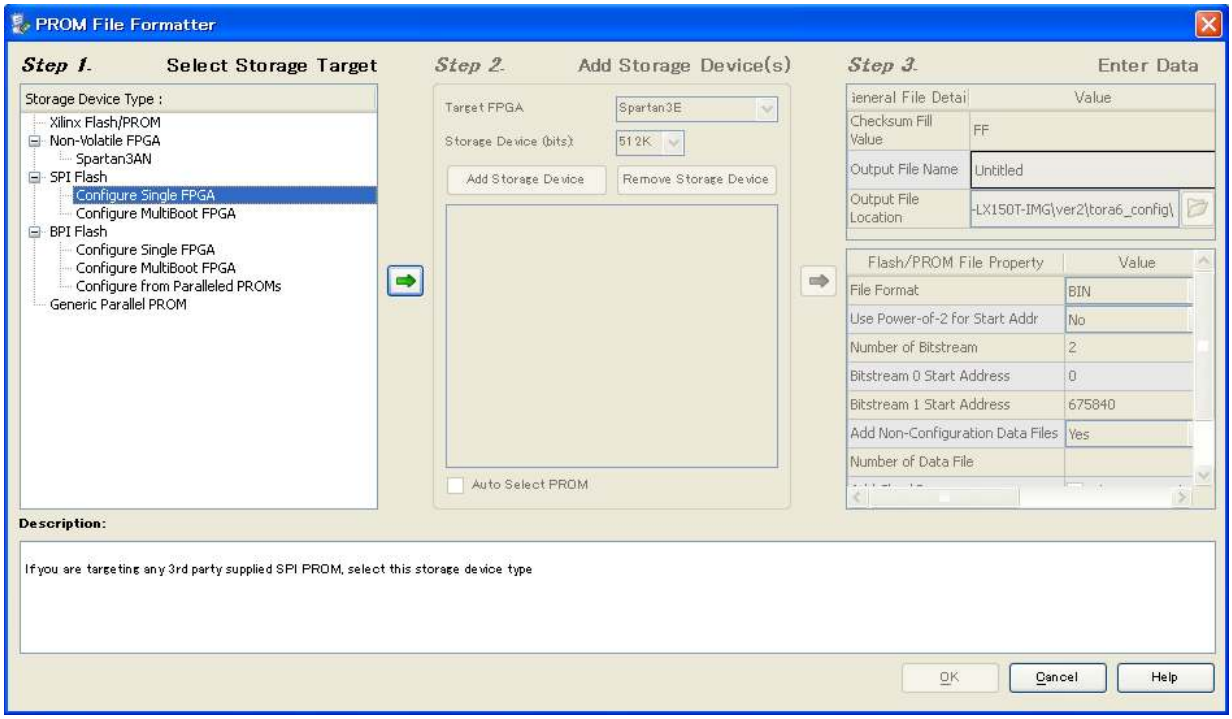


Figure 8-3 iMPACT Window 2

4. On Storage Device (bits) select **64M** and then click **Add Storage Device**.

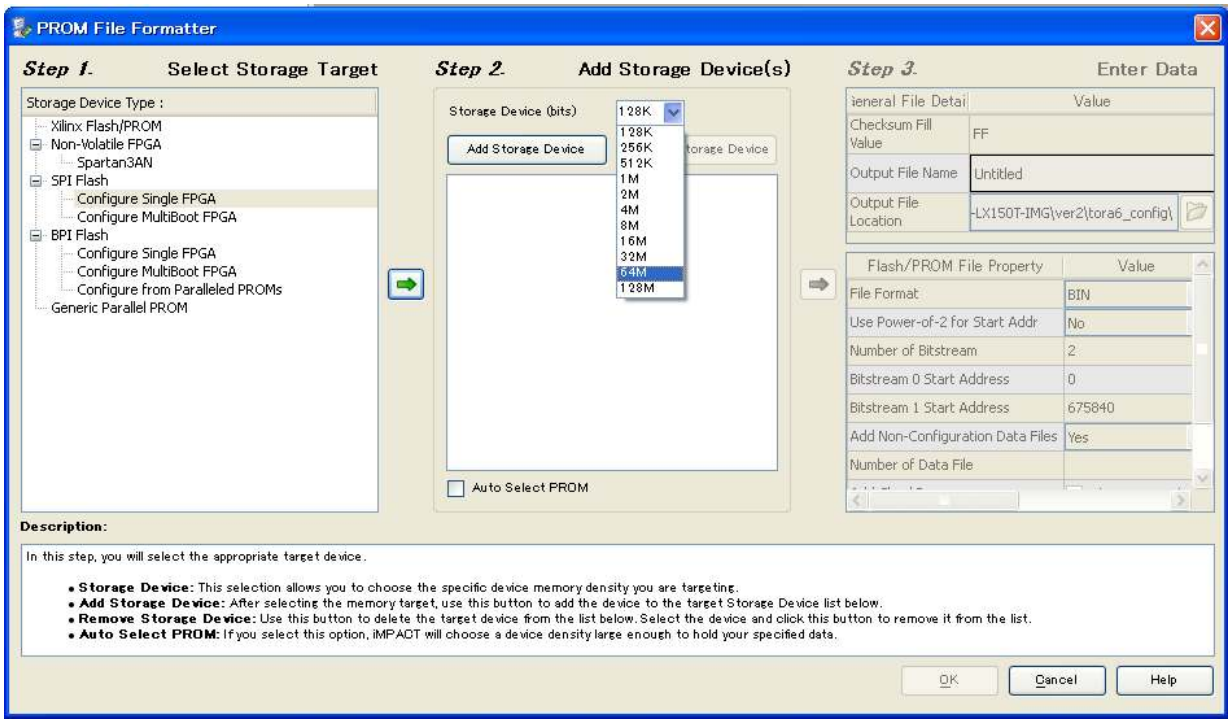


Figure 8-4 iMPACT Window 3

5. Click the right-pointing arrow. Enter a name of directory and location in the **Output File Name** and **Output File Location** fields and then click **OK**.

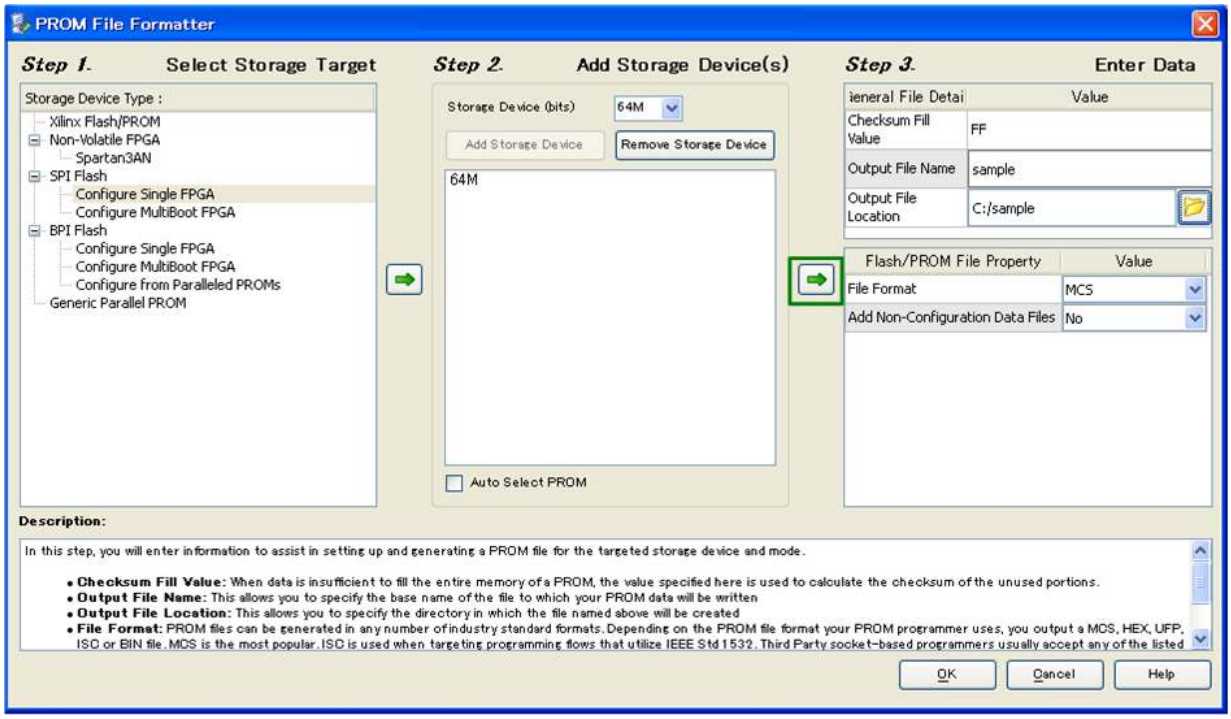

PROM File Formatter
Step 1. Select Storage Target
Storage Device Type :
Xilinx Flash/PROM
Non-Volatile FPGA
Spartan3AN
SPI Flash
Configure Single FPGA
Configure MultiBoot FPGA
BPI Flash
Configure Single FPGA
Configure MultiBoot FPGA
Configure from Paralleled PROMs
Generic Parallel PROM
Step 2. Add Storage Device(s)
Storage Device (bits)
64M
Add Storage Device
Remove Storage Device
64M
Auto Select PROM
Step 3. Enter Data
ieneral File Detai
Value
Checksum Fill Value
FF
Output File Name
sample
Output File Location
C:/sample
Flash/PROM File Property
Value
File Format
MCS
Add Non-Configuration Data Files
No
Description:
In this step, you will enter information to assist in setting up and generating a PROM file for the targeted storage device and mode.
• Checksum Fill Value: When data is insufficient to fill the entire memory of a PROM, the value specified here is used to calculate the checksum of the unused portions.
• Output File Name: This allows you to specify the base name of the file to which your PROM data will be written
• Output File Location: This allows you to specify the directory in which the file named above will be created
• File Format: PROM files can be generated in any number of industry standard formats. Depending on the PROM file format your PROM programmer uses, you output a MCS, HEX, UFP, ISC or BIN file. MCS is the most popular. ISC is used when targeting programming flows that utilize IEEE Std 1532. Third Party socket-based programmers usually accept any of the listed
OK
Cancel
Help

Figure 8-5 iMPACT Window 4

6. Click **OK**.

Figure 8-6 iMPACT Window 5

7. Select a bit file to create a configuration file.

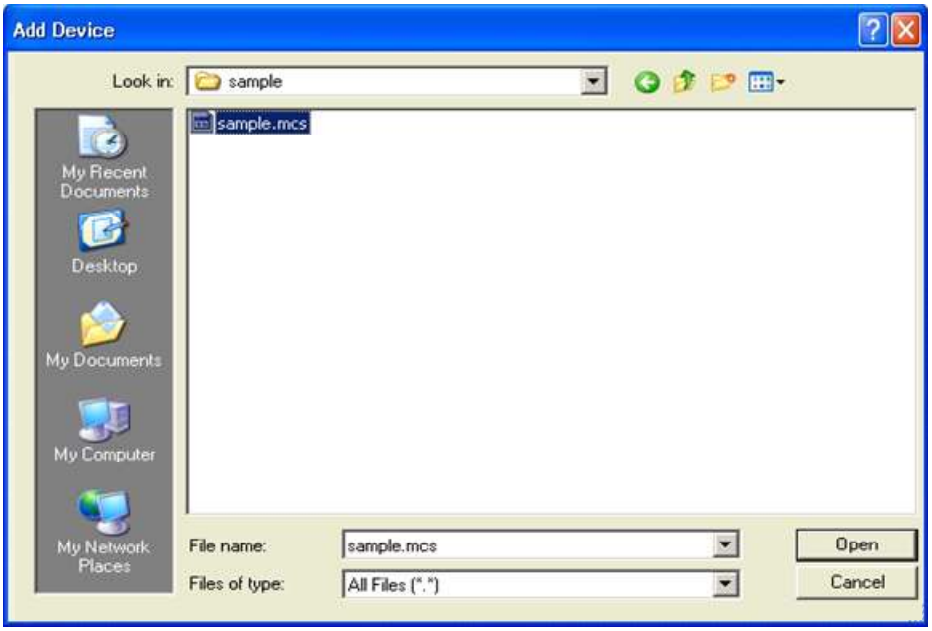


Figure 8-7 iMPACT Window 6

8. Click **No**.

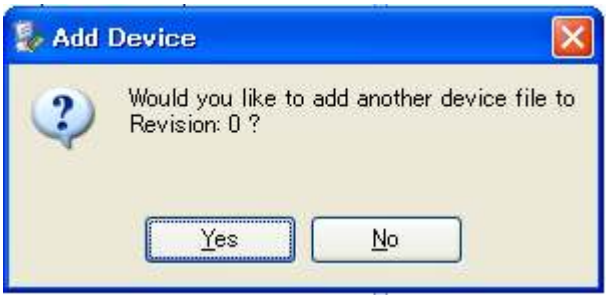


Figure 8-8 iMPACT Window 7

9. Click **OK**.

Figure 8-9 iMPACT Window 8

10. Double-click **Generate File**.

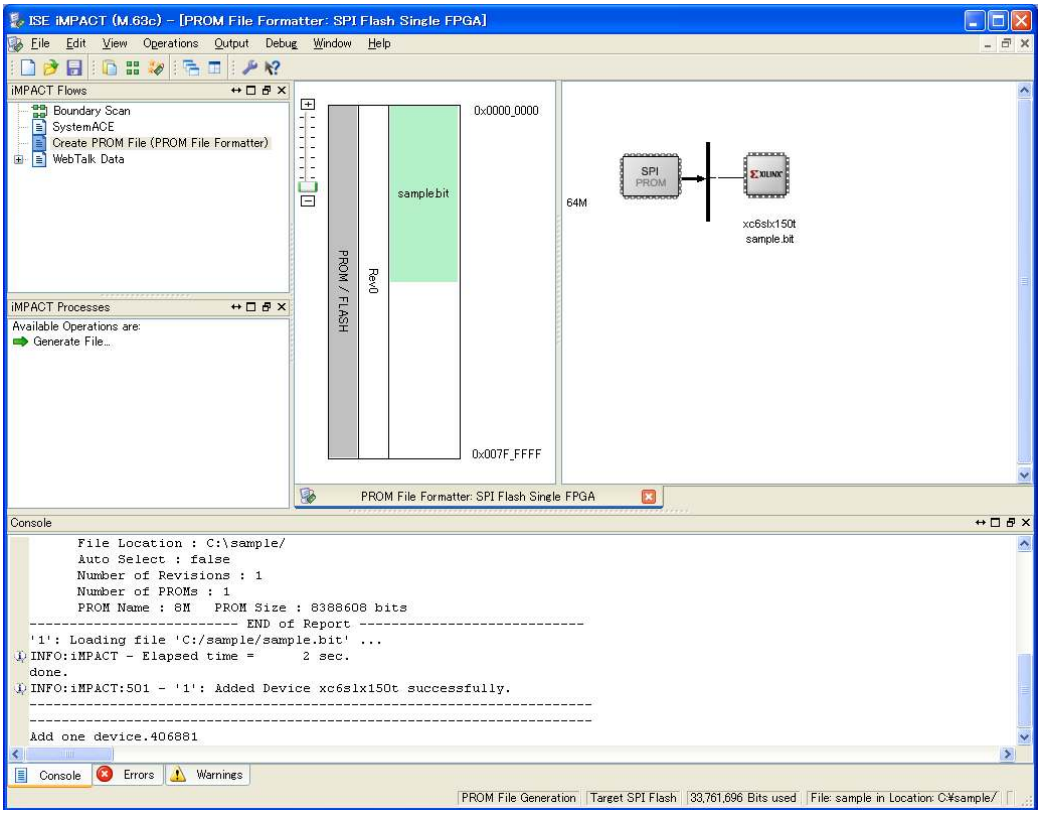


Figure 8-10 iMPACT Window 9

11. If the configuration file has been successfully created, a message **PROM File Generation Succeeded** will appear.

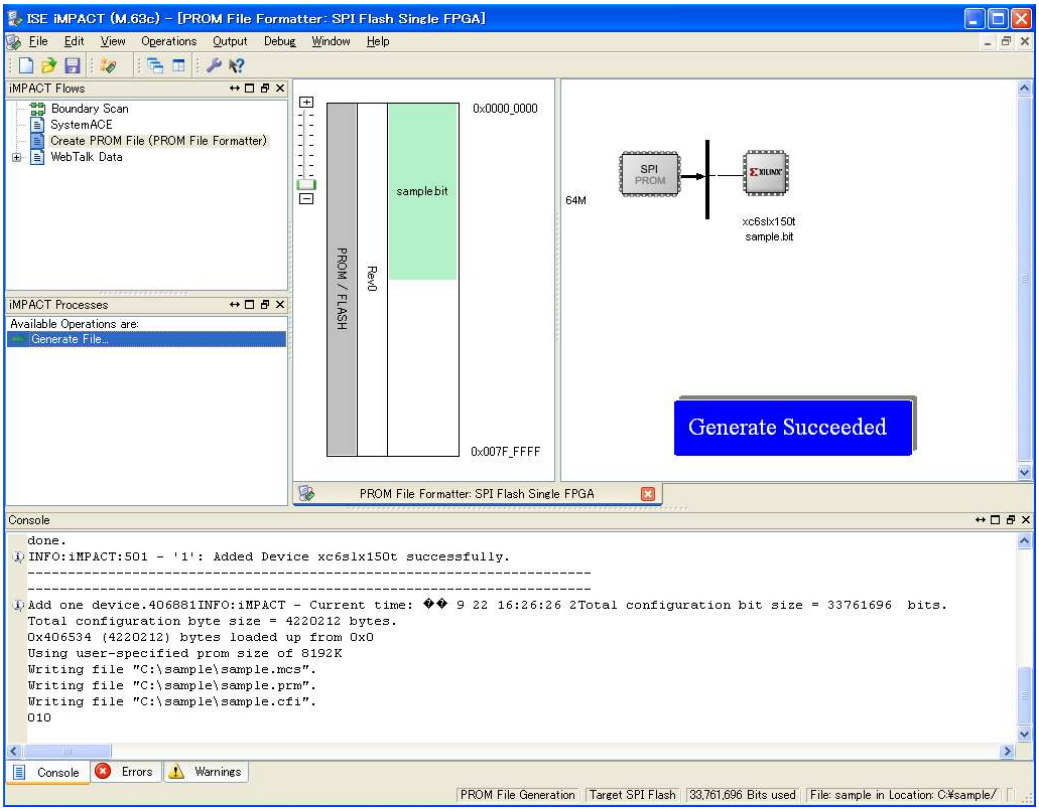


Figure 8-11 iMPACT Window 10

8.2. Writing a Configuration File into the Flash Memory

Connect a Platform USB cable to the JTAG connector (CN3) as shown in Figure 8-13. After powering on the board, start the ISE iMPACT applicaton and write a configuration file into the Flash memory by following the procedure described below.

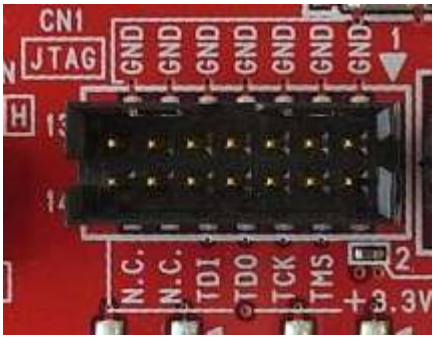


Figure 8-12 Onboard JTAG Connector

1. Double-click **Boundary Scan** and then click **Initialize Chain** shown by the arrow.

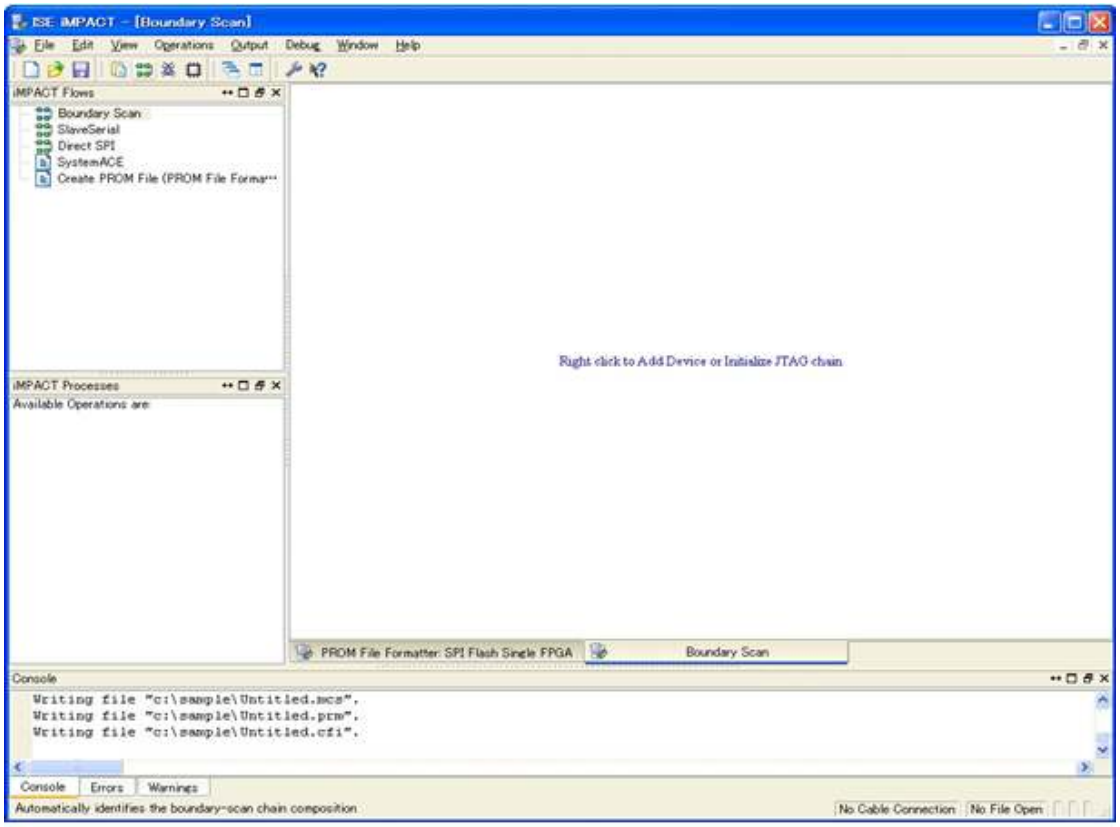


Figure 8-13 Writing into the Device 1

2. A bit/jed file configuration window will appear. Cancel it.
   Select an FPGA and right-click to select **Add SPI/BPI Flash…**.

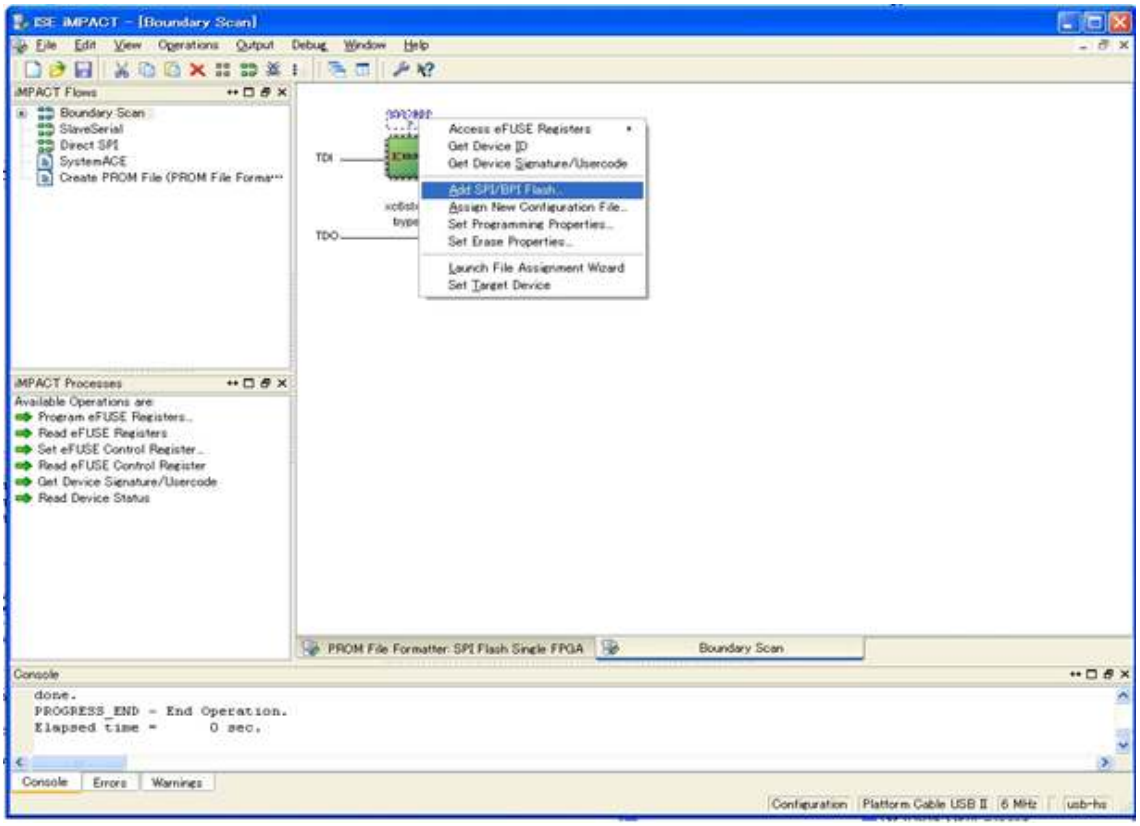


Figure 8-14 Writing into the Device 2

3. Select a configuration file (xxx.mcs) to write into the Flash memory.

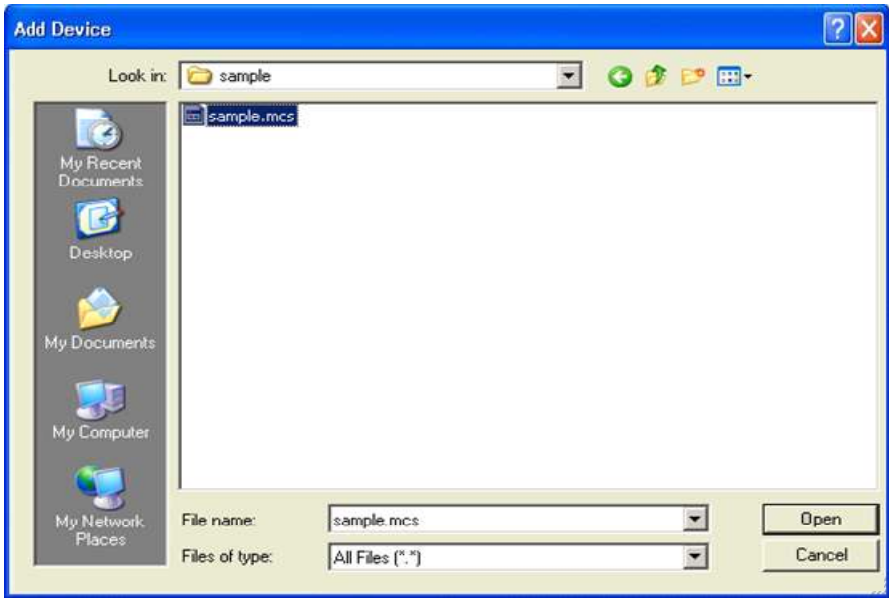


Figure 8-15 Writing into the Device 3

4. Select the onboard Flash **M25P64** and click **OK**.

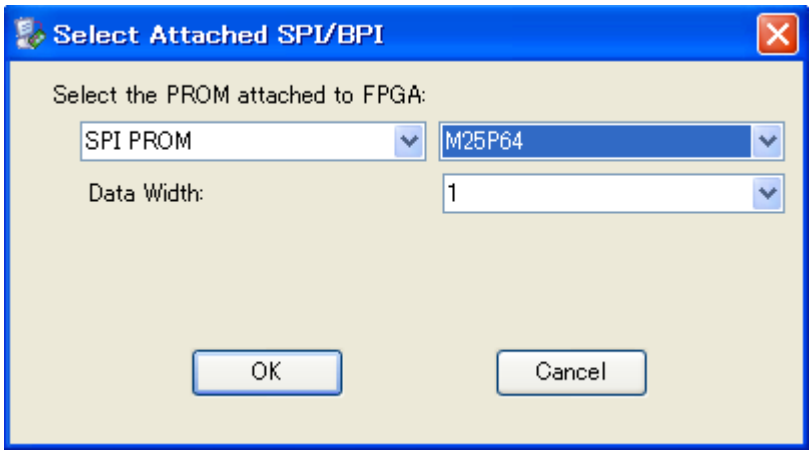


Figure 8-16 Writing into the Device 4

5. On the **iMPACT Processes** window double-click **Program**.

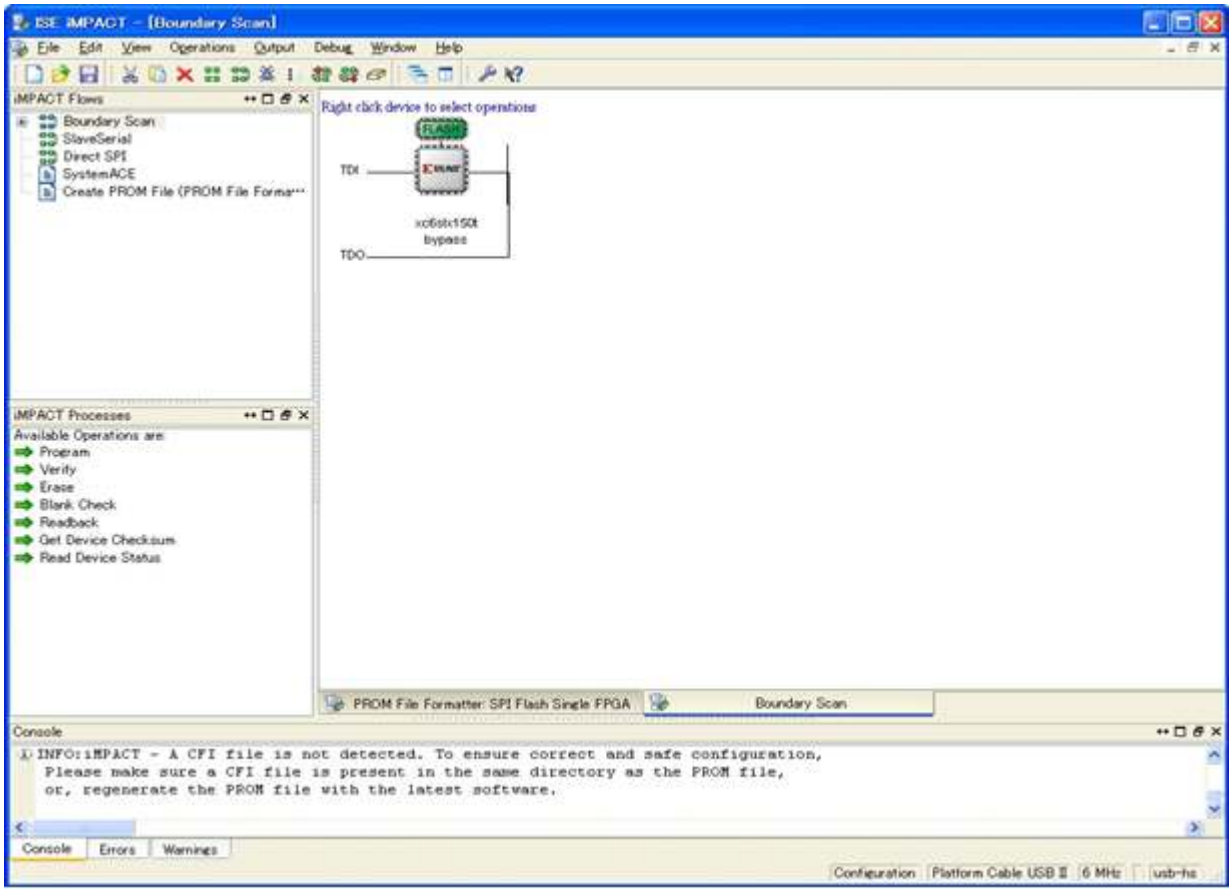


Figure 8-17 Writing into the Device 5

6. Click **OK**.

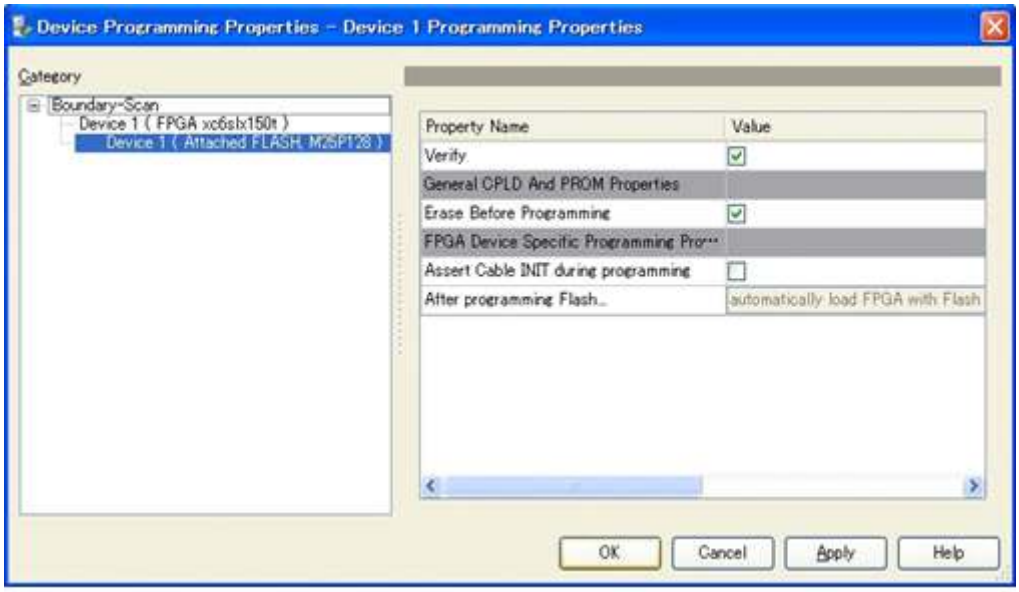


Figure 8-18 Writing into the Device 6

7. The write operation into the Flash memory will start.

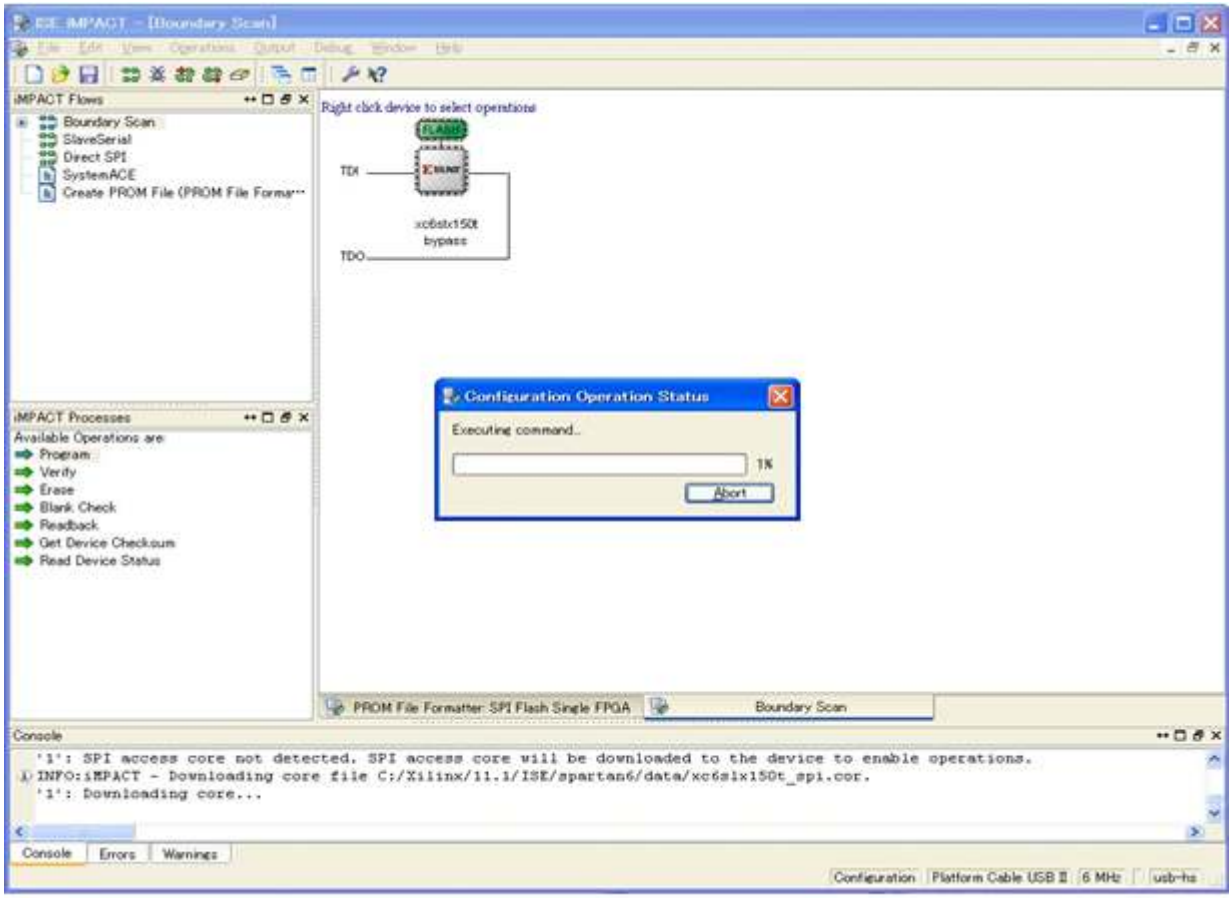


Figure 8-19 Write into the Device 7

8. If the write operation into the Flash memory is successfully completed, a message **Program Succeeded** will appear.

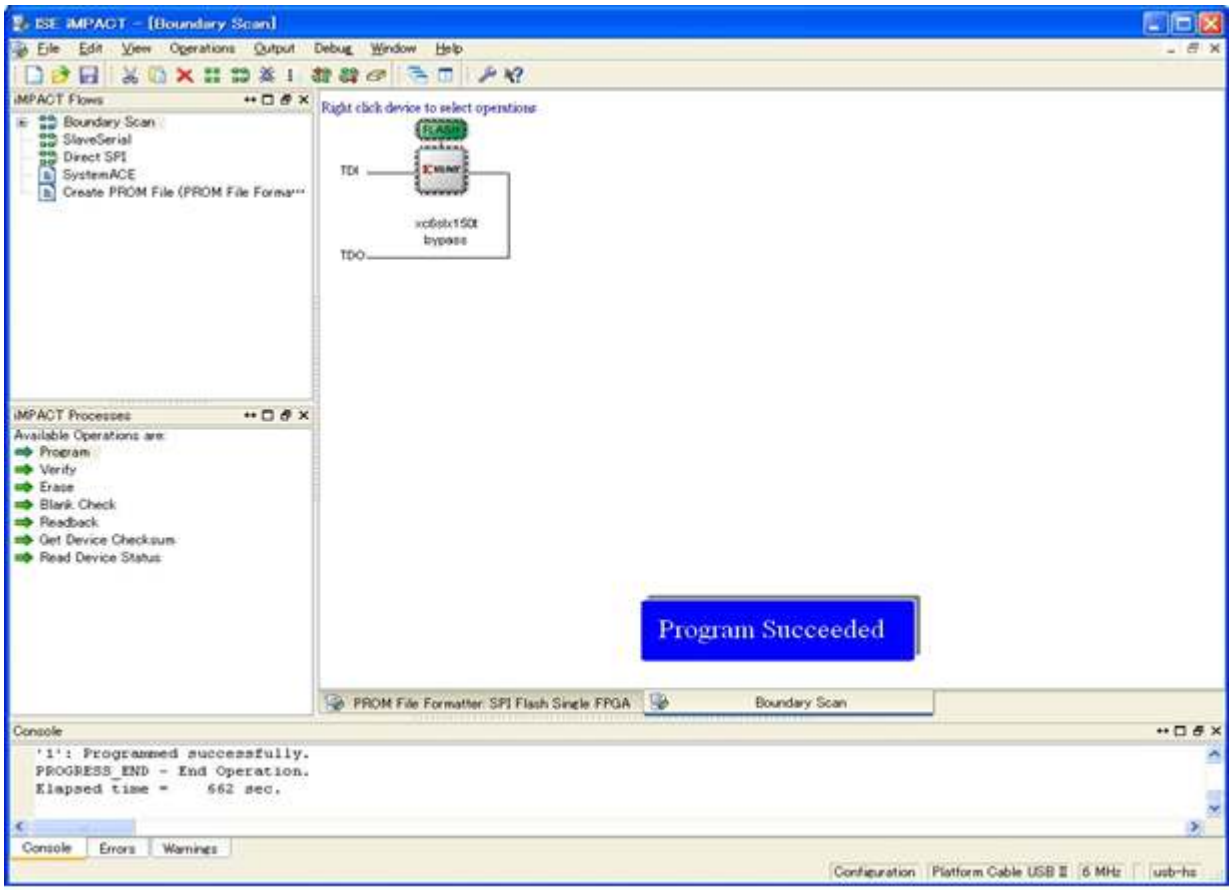


Figure 8-20 Write into the Device 8

9. The data written in the Flash memory device is used for FPGA configuration using Master-SPI. The FPGA configuration can be initiated either by turning on the power switch of the board or holding down the reconfiguration switch (SW2) for more than two seconds (see Figure 8-21 below).

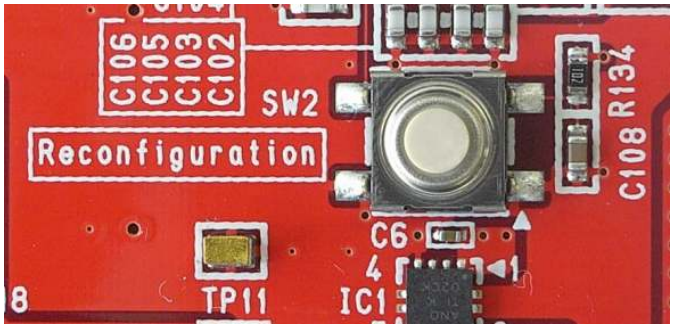


Figure 8-21 Reconfiguration Switch

10. The board provides two LEDs (15 and 16) for configuration status monitoring (see Figure 8-21 below).
Green LED15 indicates that the configuration process has been successfully completed.
Red LED16 indicates that the configuration process is in progress or failed.

Figure 8-22 Configuration Status

8.3. Configuration Time

Time required to load configuration data into the Flash memory device can be changed by setting the configuration clock on ISE Tool.
Due to the operational frequency of SPI-Flash, select 16MHz or below.

Method:

1. Right-click **Generate Programming File**
2. Choose **Process Properties**
3. Choose **Configuration Options**
4. Change the **Value** of **Configuration Rate**.
   Configuration Clock Frequency (MHz) Setting

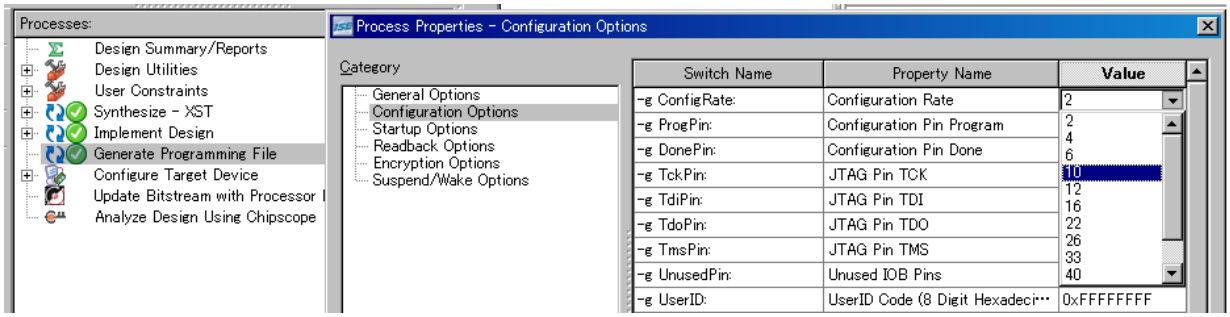


Figure 8-23 Changing Configuration Time

Target for Configuration Time:

Configuration Rate = 2MHz: Configuration Time = approx. 17 seconds
Configuration Rate = 10MHz: Configuration Time = approx. 6 seconds

8.4. Factory Switch and Jumpper Settings

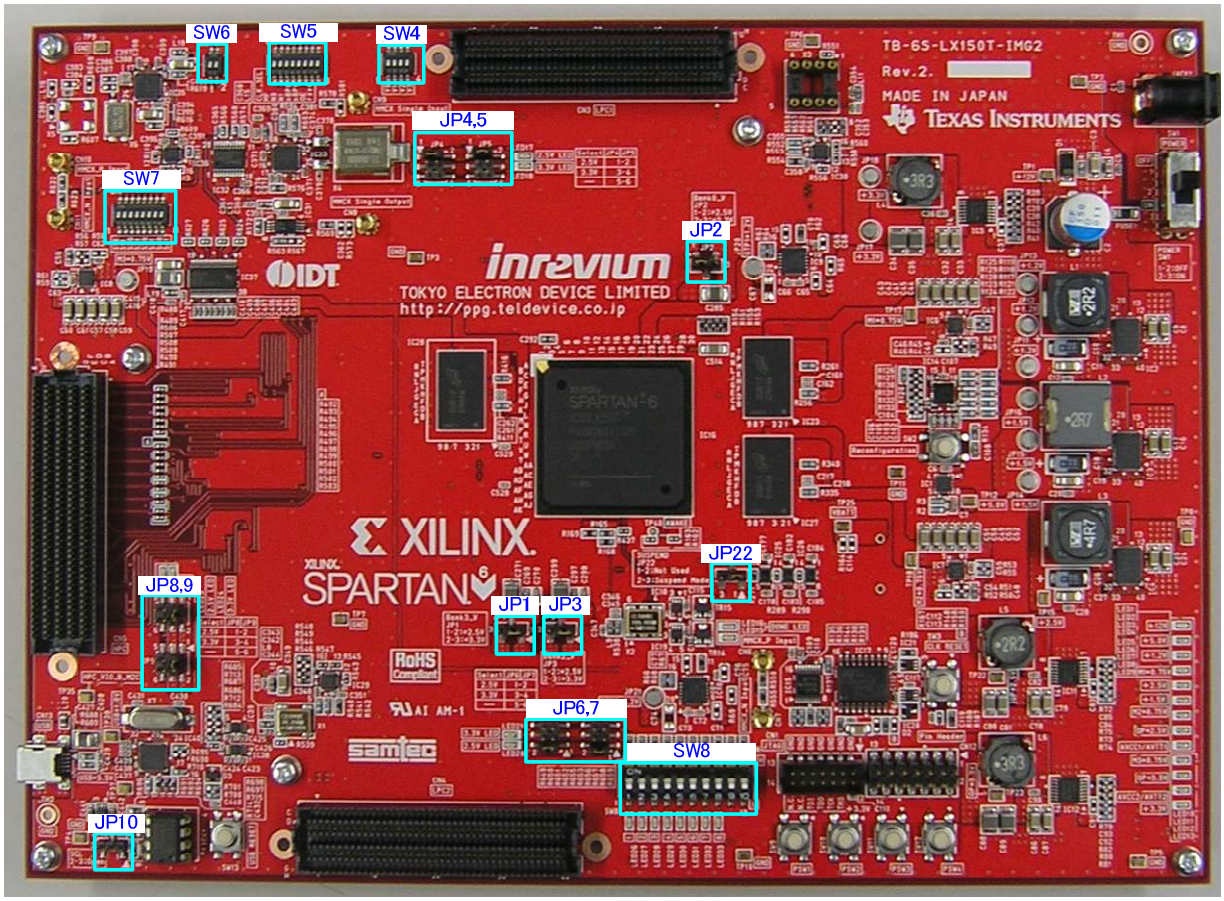


Figure 8-24 positions

Table 8-1 Initial settings

No.	Silk No.	Initial Setting	Function
1	SW4,5	ALL OFF	Setting for Video Clock
2	SW6,7	ALL OFF	Clock select setting
3	SW8	ALL OFF	User Dip SW
4	JP2	1-2	Bank0 IO Power setting (**2.5V** / 3.3V)
5	JP3	1-2	Bank2 IO Power setting (**2.5V** / 3.3V)
6	JP1	1-2	Bank3 IO Power setting (**2.5V** / 3.3V)
7	JP4,5	1-2	*FMC_LPC1 VADJ Power setting (**2.5V** / 3.3V / None)
8	JP6,7	1-2	*FMC_LPC2 VADJ Power setting (**2.5V** / 3.3V / None)
9	JP8,9	1-2	*FMC_HPC VADJ Power setting (**2.5V** / 3.3V / None)
10	JP10	1-2	Setting of serial EEPROM SCL (**Connect** / Disconnect)
11	JP22	1-2	SUSPEND Mode (Enable | **Disable**)

*__Bold character__ is factory setting.

*Setting of the two jumpers must be the same position.

™ TOKYO ELECTRON DEVICE

PLD Solution Division
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E-mail: psd-support@teldevice.co.jp

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